Original Paper

Eletrônica de Potência
Open Journal of Power Electronics

Received February 22, 2024; accepted June 18, 2024; Date of publication June 28, 2024.
The review of this paper was arranged by Associate Editor Edivan L. C. da Silva and Editor-in-Chief Heverton A. Pereira.

Digital Object Identifier http://doi.org/10.18618/REP.2005.1.037044

Proposal for a Hybrid Cycloconverter with Three-phase Input and Single-phase Output with Low Output Voltage Harmonic Distortion

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ABSTRACT This paper presents a proposal for a Hybrid Cycloconverter with Three-phase Input and Single-phase Output with Low Output Voltage Harmonic Distortion (THD_V). The proposed topology is based on the series association of Thyristor-based Cycloconverter with a non-isolated two DC-DC converters. The DC-DC converters are designed to process the minimum amount of energy necessary to mitigate harmonic distortion of the output voltage and, hence, to increase power density and efficiency. Theoretical analysis is presented and corroborated by experimental results obtained with a small-scale laboratory prototype. Different operating modes are analyzed and confirm the functionality of the proposed converter.

KEYWORDS AC-AC Converter, Cycloconverter, Harmonic Distortion, Hybrid.

I. INTRODUCTION

The industrial implementation of cycloconverters became more common with the advent of the thyristor in the 1960s, and with the improvement of control technology [1]. The cycloconverters are commonly used as induction motor drive once it is possible to control the input currents and the output voltage or current at the same time [2]. The three-phase cycloconverter consists of three single-phase converters. Each single-phase cycloconverter is made with two anti-paralleled fully controlled rectification bridges, arranged according to the number of pulses to be obtained from the converter. This arrangement is also called a matrix converter allowing bidirectional operation [3]. The association of the cycloconverter with the synchronous machine can be found in systems in which very low speeds (below 10 rpm) and very high powers (20 MW, for example) are required [4]. In the case of rotating cement tubes, the typical frequency values are in the order of 5 Hz and the number of pairs of poles of the rotating machine is significant [5].

Nowadays, in AC-microgrids, as shown in [6], cycloconverters are used to operate as a power interface between RES (Renewable Energy Sources), provided by two wind turbines, the electrical grid and a PMSM (Permanent Magnet Synchronous Motor). It is interesting to observe that high voltage applications, such as offshore wind turbines, can be electronic processed by the topology of an AC-AC converter with MMC (Modular multilevel converter) and HF (high frequency) transformer [7].

In [8], the authors show that the output voltage frequency range of cycloconverters are limited generally at 1/3 (one third) the grid frequency, due to the high harmonic content and different operating modes are used to control the speed range of motors, i.e., the frequency range of the rotating unit. In sinusoidal mode for low-speed range, the machine input voltages, and therefore the rms voltages that the cycloconverter provides, are low. This mode of operation is possible if the converters do not reach their natural control limits as the rms output voltage increases. At low speeds, this generates the inconvenient of reduced power factor for the grid.

In [9], the authors state that even with a load with unitary power factor, the cycloconverter operates with power factor between 0.7 and 0.85 lagging. For improving the power factor, in [5] is proposed the trapezoidal mode for controlling the speed of a motor, which can be applied in gearless mill drives (GMD) units with low output frequency from 0.3Hz up to 6Hz and power factor about 0.84.

In [10], the authors presented a strategy concerning the harmonic mitigation from the grid side and compensating the reactive power absorbed from the grid using an active power filter. Considering the cycloconverter operation, it provides an output voltage with a series of complex harmonics, which still can increase losses and generate torque in the opposite direction. To overcome this drawback, modulation techniques, such as PWM, space vector and delta modulation can be applied, as also demonstrated in [4].

In [11], aiming at simplifying the control strategy, the authors presented an alternative solution based on a single-phase-to-single-phase step-down cycloconverter using multiwinding center-tapped transformer. When compared to other solutions, one can conclude that a reduction of around 13% of THD_V (Total Harmonic Distortion of Voltage) is achieved, however, the final THD_V of the load voltage is still high (54%). Therefore, the proposed solution would not be

the choice to mitigate the problems caused by harmonic voltage distortions in motor drive applications.

In this scenario, in this paper the authors are proposing an alternative solution consisted of a hybrid three-phase to single-phase cycloconverter with active output voltage shaping. The proposed solution is based on the series association of Thyristor-based Cycloconverter with a Non-isolated DC-DC converters obtained with the application of an active commutation cell called EIE [12]-[14]. Among the EIE topologies, the Buck EIE Inverter (portrayed in Fig. 1) and the Buck EI Converter (portrayed in Fig. 2) are the best choices for the proposed application since the inductor current and the capacitor voltage can be controlled independently.

The main feature of both converters relays on the simplified control technique which is based on the hysteresis voltage controller using a single feedback circuit. When a suitable control strategy is applied, these topologies can be classified as a voltage follower. In other words, the output voltage follows a desired reference signal. The choice for this controller is mainly because it is robust to load variations and provides very good performance during transient conditions.

In the proposed hybrid three-phase to single-phase cycloconverter, either the Buck EIE inverter or the Buck EI converter is responsible for imposing a sinusoidal voltage waveform on the load working to compensate the output voltage, either adding or subtracting voltage, as illustrated in Fig. 3. One should note that the energy processed by both converters, highlighted in red when adding voltage and, highlighted in green, when subtracting voltage, is used to obtain the sinusoidal waveform highlighted in yellow. The energy processed by Thyristor-based Cycloconverter is highlighted in blue.

In this paper, the Buck EI topology was chosen for the implementation of the proposed hybrid cycloconverter arrangement due to the following advantages:

- The Buck EI (Input Voltage Source, E – Output Current Source, I) compensator converter is advantageous compared to the Buck EIE (Input Voltage Source, E, Current source, I and Output Voltage Source, E) studied in papers [12]-[14], since it doesn't require two extra high frequency switches.
- The THDv of the proposed hybrid cycloconverter can be reduced without passive filters at its output.
- Higher efficiency of the Buck EI converter compared to Buck EIE, since the energy stored in the inductor is discharged at the load when its switch is open, in addition to presenting lower conduction and commutation losses due to the use of fewer semiconductor switches.
- The Buck EI switches voltages never exceed the source voltage, unlike the Buck EIE (in a non-multilevel application) in which the voltage at the switches can reach twice the source voltage.
- The Buck EI converter is an extremely simple converter, easy to control and with only one switch, therefore it is a convenient solution.
- The output voltage frequency is maintained constant for the tests at 22.5 Hz (37.5% of the grid frequency). The proposed topology and control system can operate at any frequency below the grid frequency, i.e., lower than 60 Hz.

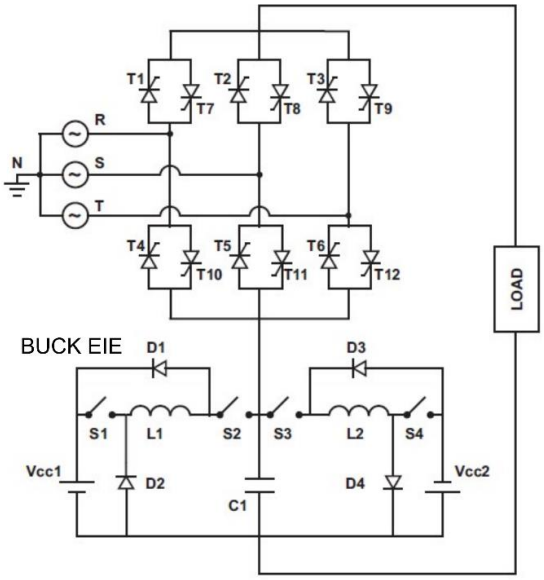


FIGURE 1. Hybrid three-phase to single-phase cycloconverter with Buck EIE Inverter.

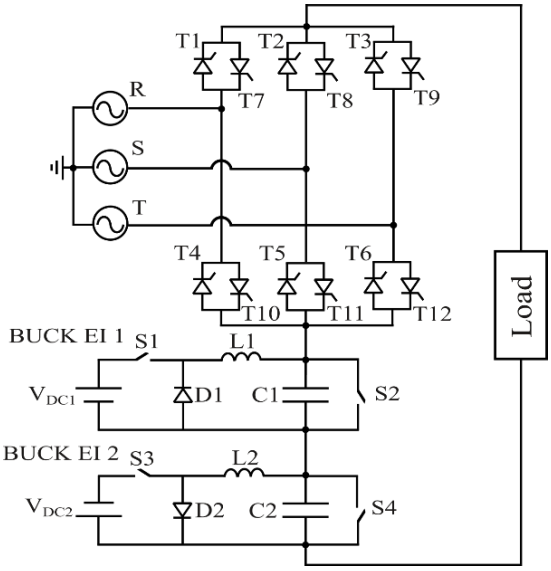


FIGURE 2. Hybrid three-phase to single-phase cycloconverter with two Buck EI Converter.

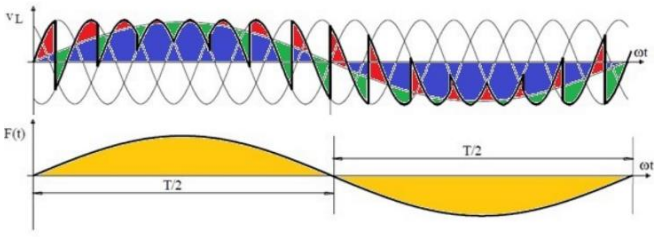


FIGURE 3. Theoretical waveforms illustrating the ratio of energy processed by each converter aiming at reducing the THD of the output voltage.

To present the obtained results, this paper is organized as follows: in Section II the authors present the proposed single-phase hybrid cycloconverter. In Section III is presented the operating principle of the proposed converter considering the positive half-cycle of the grid voltage. In Sections IV and V, the authors explain the control strategy and the Buck EI modeling, respectively. Finally, in Section V the experimental results are shown and conclusions about the

operation of the converter are discussed, including future works proposals.

II. PROPOSED CONVERTER

The single-phase hybrid cycloconverter proposed in this paper was developed considering factors such as fewer semiconductor switches, lower output voltage THD, possibility of feeding inductive loads, switches arranged for having lower voltage stress, i.e., determinant factors of efficiency and performance [14]-[17]. The most suitable topology proposal found for the series compensator was the Buck EI.

The proposed cycloconverter circuit arrangement using two Buck EI converters consists of connecting the six-pulse cycloconverter in series with the Buck EI converters, as shown in Fig. 2. The three-phase AC supplies the cycloconverter while each compensator needs a dedicated and isolated DC source.

The top-connected compensation converter (Buck EI 1) is responsible for compensating the load voltage during the positive half-cycle of the output voltage ensuring that the desired harmonic distortion threshold is respected, following the IEEE 519-2014 Standard [18]-[19]. This compensation takes place through the high frequency switch S1, for controlling the voltage across the capacitor C1, which has its voltage added to the voltage of the cycloconverter to supply the load. The same principle occurs in the negative half-cycle, but the controlled converter is the lower one, and the switch commanded to perform the compensation is S3, controlling the voltage of capacitor C2.

Switches T1 to T12 are low frequency switches, in which group T1 to T6 is responsible for conducting the entire positive half-cycle of the load current, and group T7 to T12 is responsible for conducting the entire negative half-cycle of the load voltage. Switches S2 and S4 also have low operating frequency, with switch S2 commanded to close during the negative half-cycle of the current and switch S4 commanded to close during the positive half-cycle of the load current. More details on how the structure works will be given in Section III.

III. OPERATING PRINCIPLE

Unlike the Buck EIE inverter [14], the topology of Buck EI is only capable of compensating the output voltage in one direction. For better operation of the converter, the arrangement of two Buck EI was chosen to compensate voltage in the positive and negative half-cycle, as shown in the following operating steps. Its operation is also summarized in four steps as follows.

A. *1st step – Sum of voltage in the positive half-cycle of v_t*

When the cycloconverter output voltage (V_t) is positive, it has a lower value than the reference voltage to be imposed, the Buck converter EI 1 must be able to add the voltage differential value. Figure 4 illustrates the current path of this step as well as the components that conduct it. It starts when the load voltage (V_o) becomes less than the reference voltage, during positive half-cycle. At this moment, the switch S1 is commanded to close, and during this step, the V_{DC1} source feeds the capacitor C1 through the inductor L1, which voltage is added to the cycloconverter output voltage, causing the load voltage (V_o) to reach the desired value. It is worth mentioning that switches S2 and S3 always remain open throughout this step, and switch S4 is always closed during the positive half-cycle of the load current.

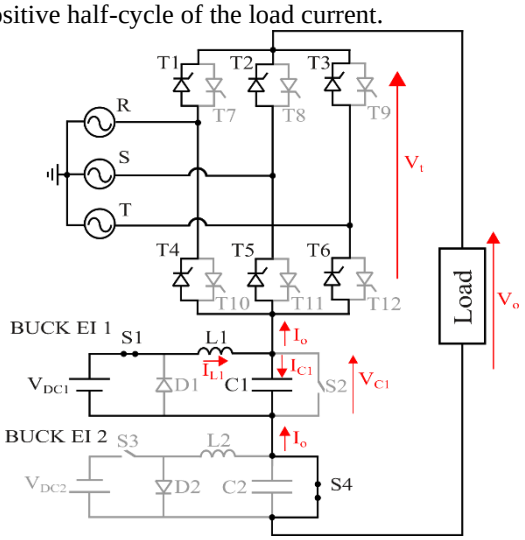


FIGURE 4. 1st step of operation: $V_o = V_t + V_{c1}$.

B. *2nd step – L1 in freewheeling*

This step occurs when the load voltage of the cycloconverter (V_t) is positive and it is not desired to increase the output voltage of the cycloconverter, since the reference voltage is lower than the voltage of the cycloconverter. Then, switch S1 opens and D1 polarizes, maintaining I_{L1} in freewheeling. Figure 5 illustrates the current path of this step as well as the components that conduct it. It starts when the load voltage (V_o) becomes greater than the reference voltage during the positive half-cycle. At this moment switch S4 remains closed, causing the load voltage (V_o) to be equal to the cycloconverter voltage V_t. It is worth mentioning that switches S2 and S3 are always remained open throughout this step, and switch S4 is always closed during the positive half-cycle of the load current.

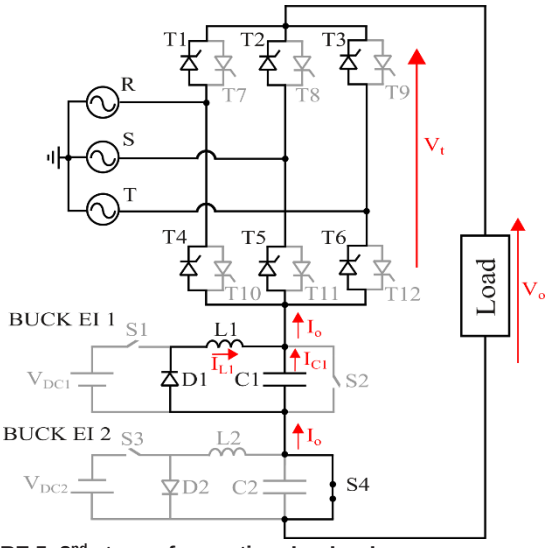


FIGURE 5. 2nd stage of operation: $I_o = I_{L1} + I_{C1}$.

C. *3rd step – Sum of voltage in the negative half-cycle of v_t*

When the cycloconverter output voltage (V_t) is negative and it has a value greater than the reference voltage to be imposed, the Buck EI 2 converter must be able to add the voltage differential value. Figure 6 illustrates the current path of this

step as well as the components that conduct it. It starts when the load voltage (V_o) becomes greater than the reference voltage, during the negative half-cycle. At this moment, the switch S3 is commanded to close, and during this step, the V_{DC2} source feeds the C2 capacitor through the L2 inductor, which voltage is added to the cycloconverter voltage, causing the load voltage (V_o) to reach the desired value. It is worth mentioning that switches S1 and S4 always remain open throughout this step, and switch S2 is always closed during the negative half-cycle of the load current.

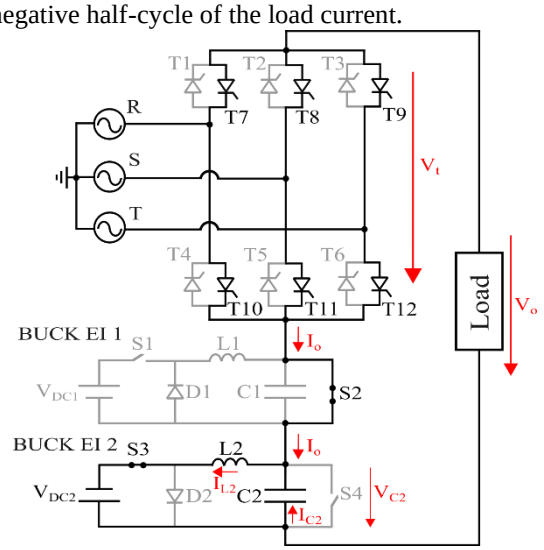


FIGURE 6. 3rd stage of operation: $V_o = V_t + V_{c2}$.

D. *4th step – L2 in freewheeling*

This step occurs when the load current of the cycloconverter is negative and it is not desired to increase the voltage of the cycloconverter, since the reference voltage is greater than the output voltage of the cycloconverter. Figure 7 illustrates the current path of this step as well as the components that conduct it. It starts when the load voltage (V_o) becomes less than the reference voltage, during the negative half-cycle. At this moment switch S2 remains closed, causing the load voltage (V_o) to be equal to the cycloconverter voltage. It is worth mentioning that switches S1, S3 and S4 are always remained open throughout this step, and switch S2 is always closed during the negative half-cycle of the load current.

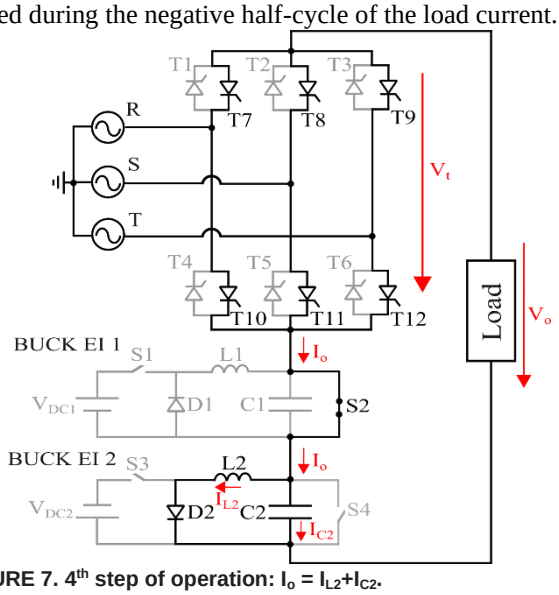


FIGURE 7. 4th step of operation: $I_o = I_{L2}+I_{C2}$.

IV. CONTROL STRATEGY

To obtain a generic control code that generates pulses for the twelve thyristors according to a desired variable reference frequency and independent of the type of load, a function was implemented in the Arduino DUE microcontroller that follows the routine presented in the flowchart of Fig. 8.

Initially, the program declares the variables to be used, defines the inputs and outputs of the microcontroller, and starts enabling the thyristors T1 and T5 when the V_{ab} signal is sampled and is synchronized with the reference voltage V_{ref}. This occurs when V_{ab} and V_{ref} pass through zero during a very close time interval, defined in the code, and both have a positive derivative. The flag variable, in this code, is responsible for storing a value that indicates which were the last thyristors in operation, i.e., which current waveform is being conducted to the load, since after being turned-on, the thyristors only block if the current that passes through them drops to zero. Thus, after synchronism and triggering of T1 and T5, the flag variable stores the value AB, which indicates that the input waveform V_{ab} is feeding the load.

The next step that the control performs is the verification of the load current half-cycle. This allows distinguishing which thyristors can turn-on and which thyristors must remain disabled. Thus, after the initialization condition, it is possible to know that the waveform it is driving is V_{ab} through the triggering of T1 and T5. As the derivative of this signal is positive, it is known that the current will be in the positive half-cycle and, therefore, thyristors T1 to T6 will be available and thyristors T7 to T12 will be blocked.

The following waveform after V_{ab} is V_{ac}, so the next thyristors to be enabled will be T1 and T6, storing the value of AC in flag. However, for this to occur, the waveform V_{ac} must be closer to the reference than V_{ab}. The calculation made by the microcontroller is the magnitude of the voltage difference between V_{ab} and V_{ref} to obtain ΔV_{ab} and similarly for the other input voltage samples: V_{ac}, V_{bc}, V_{ba}, V_{ca} and V_{cb}. Thus, after initialization, if ΔV_{ab} is smaller than ΔV_{ac}, the waveform that feeds the load is V_{ab}. As soon as this condition is reversed, T1 and T6 trigger, supplying the load with voltage V_{ac} and changing the flag value to AC.

The control continues enabling the thyristors corresponding to the V_{bc}, V_{ba}, V_{ca} and V_{cb} waveforms, respectively, as determined by the period of the reference waveform. After the positive half-cycle of the output voltage is over, the thyristors T1 to T6 are still available to start the negative half-cycle of the output voltage while the current is still positive.

Once again, the current analysis is performed and the cycle is repeated, similarly, for the negative half-cycle, however the thyristors to be triggered will now be from the negative group, T7 to T12.

Figure 9 (a) illustrates the hysteresis control logic used to drive the series compensator using two Buck EI converters and other auxiliary power semiconductor devices. The power circuit is represented in Fig. 9 (b) for better identification of the elements mentioned in the controls and the symbolic schematic of the analog control itself. This control strategy was implemented in analog electronics, using amplifiers and logic gates, as shown in Fig. 8 (a). Moreover, to limit the switching frequency and implement hysteresis control logic,

operational amplifiers were applied in the Schmitt trigger configuration.

It can be seen from Fig. 9 (a) three signals of interest for the hysteresis control logic proposed for this converter: V_{ref}, V_o and i_o. Switch S4 is commanded to remain closed while the load current i_o is in the positive half-cycle. Switch S2, in turn, is commanded dually in relation to switch S4, being enabled during the negative half-cycle of the load current i_o.

Switch S1, as demonstrated in Fig. 9 (a), is closed when the output voltage (V_o) is lower than the reference voltage V_{ref} and is opened when the output voltage is higher than the reference voltage. Furthermore, the operation of switch S1 occurs only if the waveforms of V_{ref} and load current i_o are in their respective positive half-cycle, which is controlled by "AND" logic. Switch S3 operates in a complementary way to the operation of switch S1, working with the role of compensating the load voltage V_o during the negative half-cycles of the load current i_o and the reference voltage V_{ref}. The reference signal described here is a sinusoidal signal obtained from the output voltage waveform of the cycloconverter, which is synchronized for maintaining the same phase and frequency, through a PLL (Phase-locked loop).

Switches S2 and S4 present a relatively simple control technique, in which only the load current i_o determines their states. Also operating in a dual way, switch S2 is triggered during the negative half-cycle of the current and switch S4 is triggered during the positive half-cycle of the current flowing through the load.

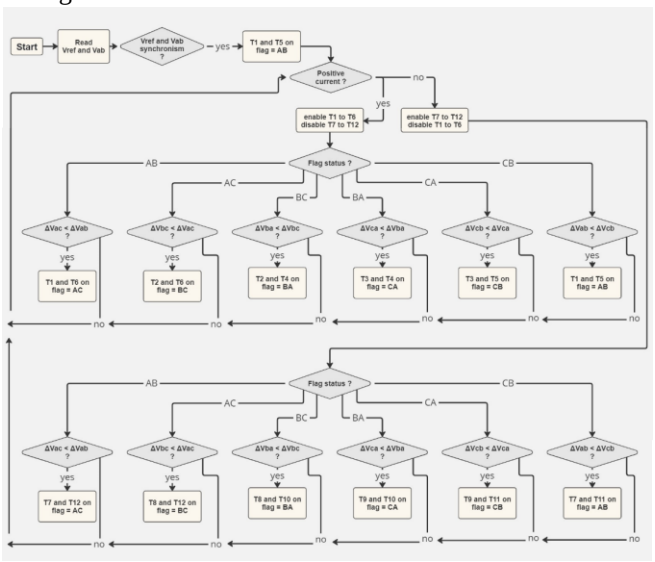


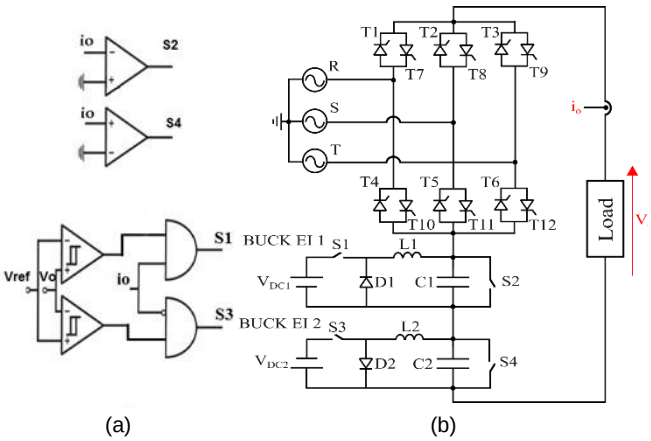
FIGURE 8. Control flowchart for cycloconverter thyristors considering variable frequency operation.

V. BUCK EI MODELING

The mathematical model that describes the Buck EI converter is based on equations (1) and (2) in the state-space representation. Therefore, it is possible to model the converter during the two operation steps, i.e., switch-on and off, resulting in an average model of the system [11].

$$\frac{dX_1}{dt} = A_1.X_1 + B_1.U_1 \quad (1)$$

$$\frac{dX_2}{dt} = A_2.X_2 + B_2.U_2 \quad (2)$$



(a) (b)

FIGURE 9. (a) Control logic for the two Buck EI converters; (b) proposed power circuit.

A. *Switch S turned-on*

The circuit representing the step in which the semiconductor S switch turned-on is represented in Fig. 10.

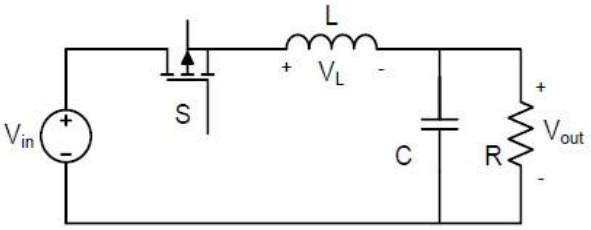


FIGURE 10. Equivalent circuit with switch S turned-on.

Applying Kirchhoff's Voltage Law (KVL) to the external loop, (3) is obtained.

$$V_L = V_{in} - V_{out} \quad (3)$$

The voltage at the inductor terminals is given by (4) as follows,

$$V_L = L.\frac{dI_L(t)}{dt} \quad (4)$$

Substituting (4) in (3), one can find the variation of inductor's current, represented in (5).

$$\frac{dI_L}{dt} = \frac{V_{in}}{L} - \frac{V_{out}}{L} \quad (5)$$

Once the capacitor losses are neglected, the load voltage is the same as the capacitor's voltage, resulting in (6).

$$\frac{dI_L}{dt} = \frac{V_{in}}{L} - \frac{V_c}{L} \quad (6)$$

Applying Kirchhoff's Current Law (KCL) is obtained (7).

$$I_C = I_L - I_R \quad (7)$$

The current flowing through the capacitor is given by (8).

$$I_C = C.\frac{dV_c}{d_t} \quad (8)$$

Substituting (8) in (7), is acquired the capacitor voltage variation, represented in (9).

$$\frac{dV_C}{dt} = \frac{I_L}{C} - \frac{V_c}{RC} \quad (9)$$

A convenient way of representing the system composed by (6) and (9) is in matrix form. With that, for the *S* switch turned-on, (10) follows.

$$\begin{bmatrix} \frac{dI_L}{d_t} \\ \frac{dV_c}{d_t} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \cdot \begin{bmatrix} I_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} . V_{in} \quad (10)$$

B. *Switch S turned-off*

The circuit that represents this stage is shown in Fig. 11.

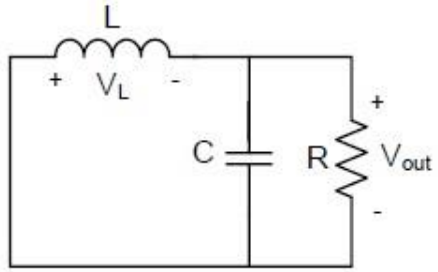


FIGURE 11. Equivalent circuit with switch S turned-off.

Applying the KVL to the outer loop, (11) is obtained.

$$V_L = -V_{out} \quad (11)$$

Substituting (4) in (11), is obtained (12).

$$\frac{dI_L}{dt} = -\frac{V_c}{L} \quad (12)$$

In (7) and (9) are repeated for the *S* switch turned-off. Therefore, is possible to arrange the matrix form of the Buck EI converter, representing the *S* switch turned-off through (13).

$$\begin{bmatrix} \frac{dI_L}{d_t} \\ \frac{dV_c}{d_t} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \cdot \begin{bmatrix} I_L \\ V_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} . V_{in} \quad (13)$$

C. *Buck EI converter average model*

From the modeling, it is observed that there are two different dynamic models related to the switching stages of the Buck EI. An average of the time switching period is performed for having a single equation that describes the system behavior [11]. Thus, (1) and (2) can be expressed through (14).

$$\frac{dX}{dt} = [A_1 . D + A_2 . (1 - D)] . X + [B_1 . D + B_2 . (1 - D)] . U \quad (14)$$

VI. EXPERIMENTAL RESULTS

A. *Modeling of Buck EI components*

The input parameters for designing the Buck EI components are presented in Table I. These parameters were considered for the experimental setup, in which the output power is 500 W. The maximum switching frequency of the hysteresis controller is 30 kHz.

TABLE I. Buck EI Parameters

Parameters	Value
Input Voltage (V_{in})	100 Vdc
Load Voltage (V_o)	60 Vdc
Maximum Switching frequency (f_s)	30 kHz
Load	7.2 Ω
Rated output power of Buck EI (P_o)	500 W
Inductor current ripple (ΔI_L)	10 %
Output voltage ripple (ΔV_{out})	5 %

For the components of the Buck EI compensator, through (15) is calculated the capacitance of C_1 and C_2.

$$C_1 = C_2 = \frac{\Delta I_L}{2 . \pi . f_s . \Delta V_{out}}$$
$$C_1 = C_2 = \frac{0.5 * 8.333}{2 * \pi * 30k * 0.05 * 60} = 7.358\ \mu F \quad (15)$$

The commercial value of 12 μF was adopted for the simulations and used in the experimental setup. Following in (16), it is required to calculate the duty cycle "D" so that the Buck EI inductors L1 and L2 remains in continuous conduction mode (CCM). Then, in (17) is calculated the inductance of both converters.

$$D = \frac{V_{out}}{V_{in}} = \frac{60}{100} = 0.6 \quad (16)$$

$$L = \frac{V_{out} . (V_{in} - V_{out})}{V_{in} . \Delta I_L . f_s}$$
$$L = \frac{60 . (100 - 60)}{100 * 0.5 * 8.333 * 30k} = 192\ \mu H \quad (17)$$

In practice, was adopted an inductor with a higher value than the one calculated with equation (3). This is done to guarantee the CCM throughout the converter's operating range. For this reason, will be adopted L = 450 µH. Table II summarizes the components designed for 60% duty cycle and respective semiconductors employed in the experimental setup.

TABLE II. Components designed for 60% duty cycle

Components	Value
Capacitor	12 µF
Inductor	450 µH
Diodes	MUR4100E
MOSFET	IRFP460

B. *Implemented Prototype*

The six-pulse cycloconverter, shown in Fig. 12, was designed to operate with mains input frequency of 60 Hz, being powered by a three-phase source of 220 Vrms. The topology of the three-phase AC-AC converter is a conventional one for three-phase input and single-phase output constituted by twelve SCR of 25 A and 800 V (model MCR25N), to avoid excessive heating of these devices during the tests, with a thermal dissipator of 6 cm x 6 cm x 13 cm.

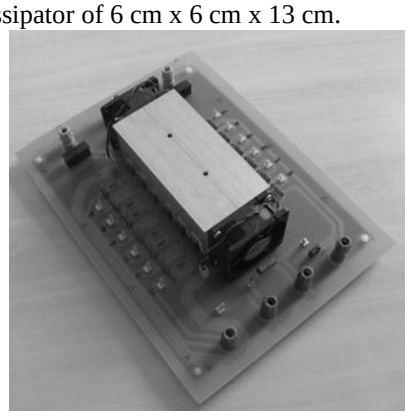


FIGURE 12. Six-pulse cycloconverter printed circuit board with three-phase inputs and single-phase output.

For the Buck EI converter, it was possible to specify the passive components for the desired voltage and current

variations (voltage and current ripple) at the converter's output. Figure 13 illustrates the converter board developed with the analog control coupled to the power circuit. Resistors that do not have a power class are conventional ¼ W resistors.

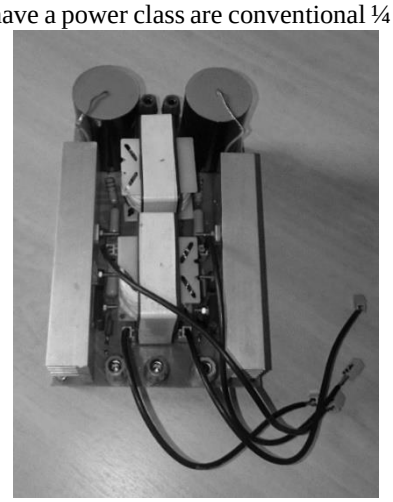


FIGURE 13. Buck EI Compensator Converter Board.

C. *Hybrid Cycloconverter operation – Cycloconverter and Buck EI series compensator*

For all tests, the reference sinewave was adjusted to 22.5 Hz. Figure 14 presents the output voltage of the hybrid cycloconverter in green, with THD_v of 9.848%, the cycloconverter output voltage in purple, with THD_v of 28.854% and the Buck EI output voltage shown in blue. It is noticeable that with a small contribution from the compensation converter, the output waveform (in green) is close to the sinusoidal format with 66% of reduction in the THD_v. This was achieved for Buck EI compensator processing only 12.5% of the total output power.

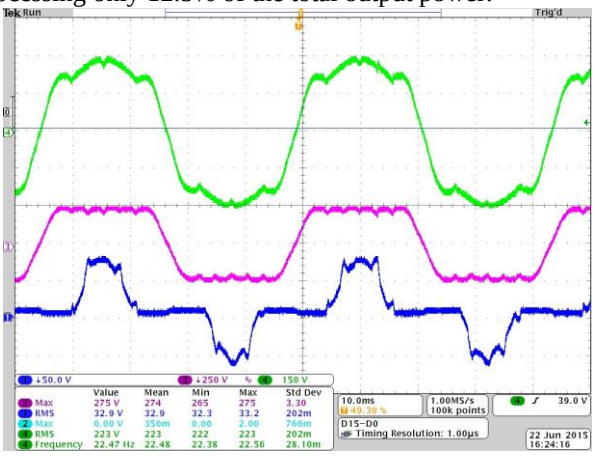


FIGURE 14. Hybrid Cycloconverter voltage in green, output voltage of the cycloconverter in purple and compensation output voltage in blue.

Figure 15 adds to the previous results the reference voltage waveform, in blue, synchronized with the cycloconverter voltage, in purple, which is delivered to the control for comparison with a sample of the output voltage. This strategy allows the definition of control pulses and the correct imposition of the desired output voltage, which is illustrated in green.

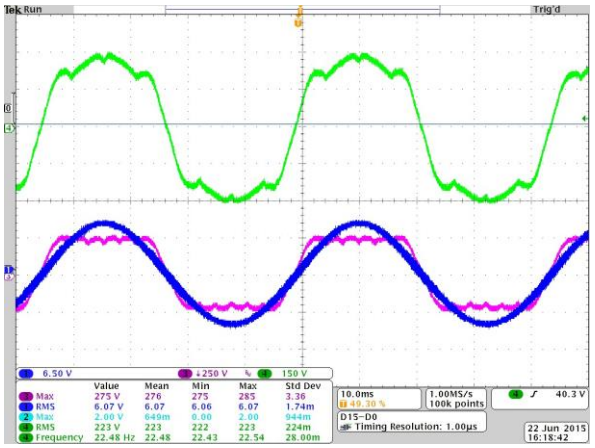


FIGURE 15. Hybrid Cycloconverter output voltage in green, reference voltage in blue and, cycloconverter output voltage in purple.

Figure 16 illustrates the hybrid cycloconverter output voltage, shown in green, and current results for a slightly inductive load, with power factor of 0.934 lagging. It is possible to observe the influence of voltage compensation on the output current i_o, in purple. Figure 17 shows the same voltage and current results for the same load, however, without voltage compensation, that is, without the action of the Buck EI converters. This result shows that the voltage across the RL load is equal to the six pulses cycloconverter output voltage.

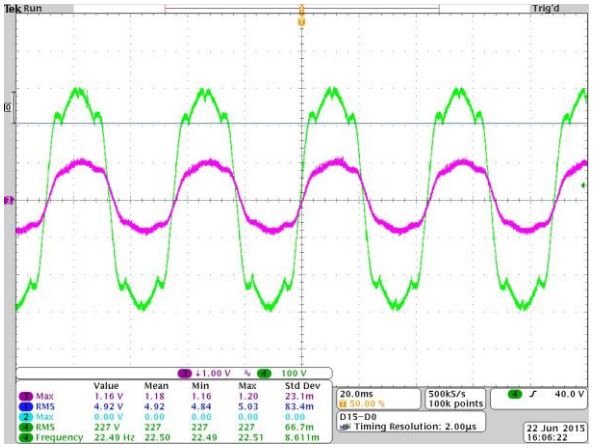


FIGURE 16. Hybrid cycloconverter compensated output voltage, in green, and current (RL load) of cycloconverter.

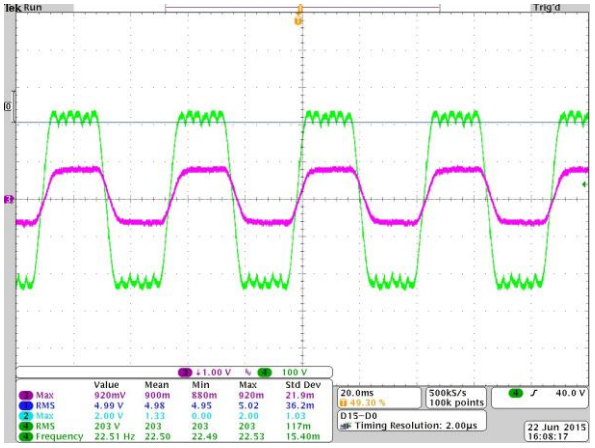


FIGURE 17. Hybrid cycloconverter output voltage, in green, and current, in purple, without compensation action of the two Buck EI converters (RL load).

Regarding the voltage stress supported by the semiconductor switches of the Buck EI converters, Fig. 18 shows their waveforms, in purple, accompanied by the gate signals, in light blue, for a short time interval for Buck EI 1 (switch S1) and Fig. 19 shows the results for Buck EI 2 (switch S3). The voltage stress levels are limited to the input voltage.

FIGURE 18. Voltage across Buck EI 1 switch (S1), in purple, and respective control signals, in light blue.

FIGURE 19. Voltage across Buck EI 2 switch (S3), in blue, and respective control signals, in green.

D. *Control signals*

Following, are presented the results of tests that validate the implemented control strategy regarding the generation of a sinusoidal reference using a PLL, generation of the trapezoidal waveform of the cycloconverter with six pulses and generation of high frequency pulses for the compensator switches.

To validate the PLL algorithm, which is necessary for generating a reference voltage synchronized with the fundamental component of the hybrid cycloconverter output voltage, it was evaluated the synchronism between the sample of the AC-AC converter output voltage and the output signal of the microcontroller's digital pins.

Figure 20 shows the digital PWM output signal of the microcontroller after passing through a first-order low-pass filter (sinusoidal waveform, in pink) against the output voltage of the cycloconverter, in green. Comparing the half-cycles of the cycloconverter output voltage and the logic level of digital PWM that generates a sinusoidal reference, it is concluded that the PLL was effective in generating a synchronized sinusoidal reference.

The sample of the output waveform of the cycloconverter has its amplitude normalized to the range of microcontroller and, at this stage, even with the use of low-pass filters, this signal has a noise that must be considered by the microcontroller. Note that the presence of noise in the supply voltage causes numerous zero crossings in the pin named "GPIOa". The logic level of this pin is conditioned to the supply voltage zero-crossing. On the other hand, the "GPIOa" pin is conditioned to the zero crossing of the PLL output signal. As there were no signal changes during the zero-crossing in the "GPIOa"' pin, it is guaranteed that the PLL operates efficiently in generating a purely sinusoidal signal, which is synchronized with the fundamental of the cycloconverter's voltage, even if it presents harmonic and/or noise.

Figure 20 also shows the high frequency pulses that are delivered to the two Buck EI converters. These pulses are generated by comparing the output voltage sample V_O with the sinusoidal reference V_{ref} obtained by the PLL. In this figure, it is possible to observe the operation of the simple control strategy developed. For the positive half-cycle of V_o and when V_o is lower than V_{ref}, switch S1 turns-on, as shown in light blue waveform of Fig. 20, controlling the voltage V_{C1}. For the negative half-cycle of V_o and when V_o is higher than V_{ref}, switch S3 turns-on, as shown in dark blue waveform of Fig. 20, controlling the voltage V_{C3}.

The proposed compensator features an almost instantaneous compensation response due to the hysteresis control. Once the switching frequency is variable, the maximum frequency achieved was 30 kHz.

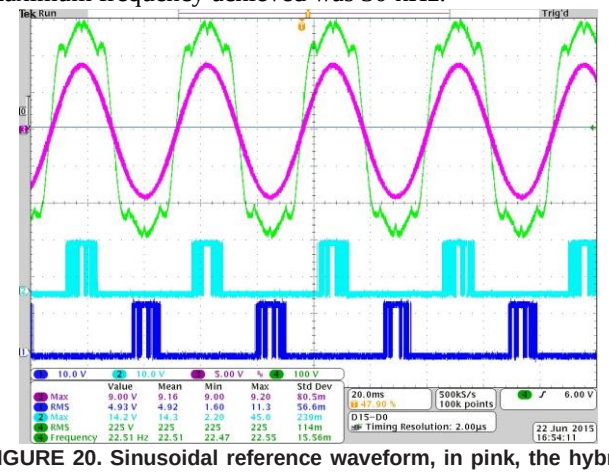


FIGURE 20. Sinusoidal reference waveform, in pink, the hybrid cycloconverter output, in green, and compensator control pulses, in light blue (operation of switch S1) and dark blue (operation of switch S3).

Figure 21 shows the control pulses of the auxiliary switches S2 and S4 of the compensation converters (Buck EI). As it's possible to observe, such switches are controlled by the load current half-cycles, therefore, they work in a complementary way. In other words, switch S2 is turned-on for the negative half-cycle of load current i_o, while S4 is turned-off. The opposite occurs when the i_o is in the positive half-cycle. They operate at the load current frequency, i.e., 22.5 Hz. Moreover, it is shown the output voltage in green and, in pink, the output current for a RL load.

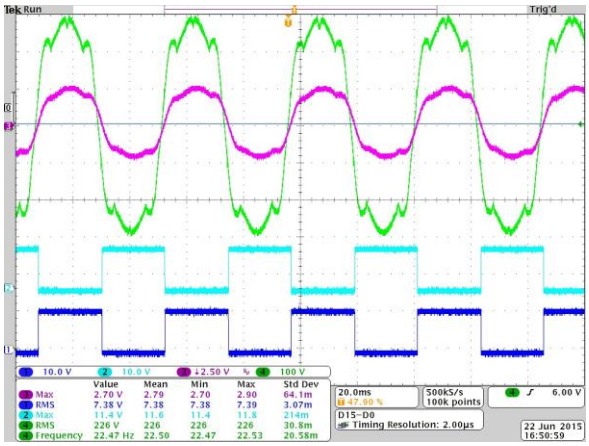


FIGURE 21. Sinusoidal reference waveform, in pink, hybrid cycloconverter output voltage, in green, and compensator control pulses, in light (operation of switch S1) and dark blue (operation of switch S3).

The control pulses of twelve thyristors that composes the cycloconverter (T1 to T12) are generated in Arduino microcontroller according to the control strategy explained previously. Figure 22 shows the control pulses for the twelve SCR's and the cycloconverter output voltage waveform, in green, resulted from these pulses.

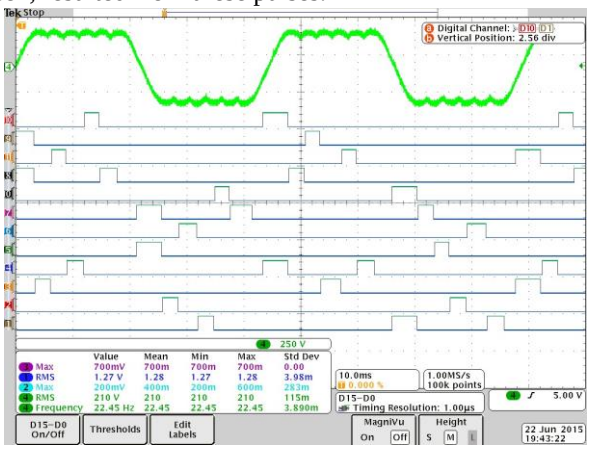


FIGURE 22. Cycloconverter output voltage waveform in green and control pulses for thyristors T1 to T12.

E. *Results for Increased V_o Voltage Compensation*

For further improvement of quality of the voltage waveform delivered to the load, was implemented a test with a higher level of compensation. For achieving this, the series compensator processed, approximately, 25% of the output power. Figures 23 and 24 confirm this improvement by presenting the voltage that feeds the load, in blue. In Fig. 22, it is observed the output frequency of 22.56 Hz. One can observe that the result approaches, approximately, a sinusoid further reducing the harmonic content, which is 5.8%, slightly higher than the limits established by IEEE Std 519-2014 [14]. For higher series compensation of the output voltage, it is required to drain more power from Buck EI compensator, which improves the output voltage THD_v.

Figure 24, in turn, shows the results of voltage and current in the load, also comparing the reference voltage with the output voltage of the cycloconverter. Once again, it is possible to verify the effective synchronism of these waveforms that allow the compensation converters to operate at the right time validating the proposed hybrid structure.

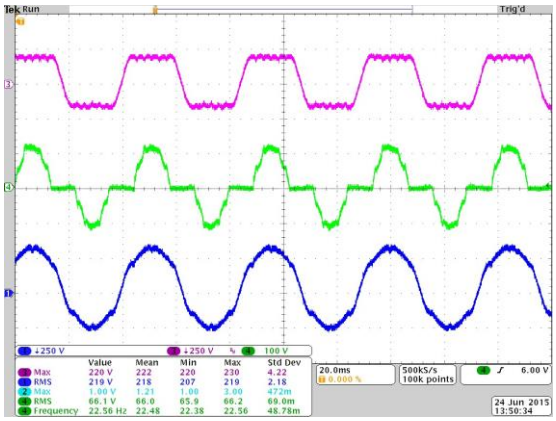


FIGURE 23. Voltage waveform of cycloconverter, in pink, compensation output voltage in green, and at the output load voltage, in blue.

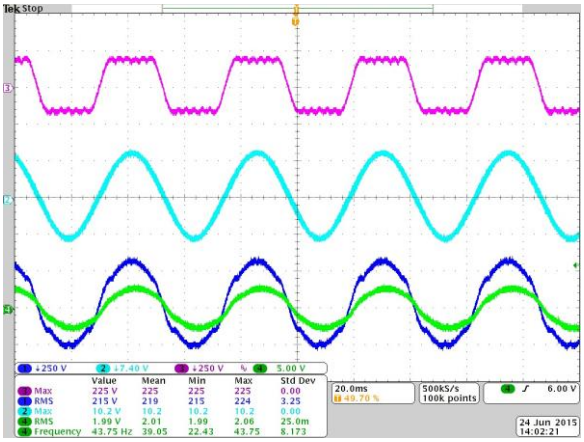


FIGURE 24. Cycloconverter voltage in purple, reference voltage, in light blue, output voltage, in blue, and current, in green.

In Figure 25, is presented the Fast Fourier Transform (FFT) result of the six pulse cycloconverter output voltage, in green, and the load output voltage, in red. It is possible to observe that for higher frequencies than fundamental (22.5 Hz), the load output voltage presents lower harmonic amplitudes (THD_V of 5.8%).

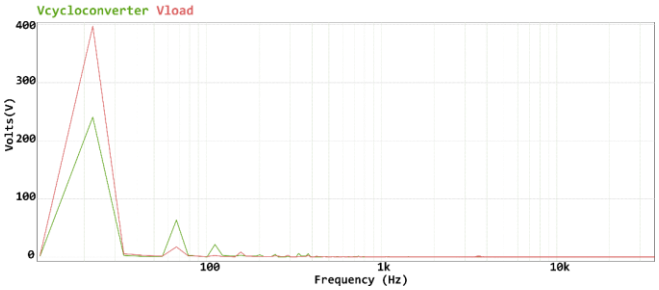


FIGURE 25. FFT results for the six pulse cycloconverter output voltage, in green, and the load output voltage, in red.

VII. CONCLUSIONS

In this paper, was presented the hybrid circuit arrangement, composed by the cycloconverter with three-phase inputs and single-phase output of six pulses in series with a compensation converter, i.e., two conventional Buck EI converters. The proposed topology stands out for its low level of output voltage harmonic distortion, without the need of passive filters at the converter's output. In addition, low level of voltage stress in switches and diodes, the use of a simple, efficient, and low-cost control strategy, high speed dynamic response and its robustness are outstanding characteristics. Experimental results were presented, demonstrating the

operational flexibility of the proposal, and confirming its operational characteristics.

It was possible to identify, in practice, that the proposed converter operates with voltage imposition, through a simple, efficient, and low-cost control strategy. It was also verified that the output voltage presents low harmonic distortion, under different load conditions, processing, for this, a small amount of power compared to the cycloconverter, thus promoting its robustness and efficiency. Finally, the aim of this paper was to show the feasibility of having a low power DC-DC converter associated with a high power cycloconverter to reduce the output voltage THD. The single-phase hybrid cycloconverter proved, for all cases, to operate as expected.

Other topics discussed during the development of this work, but which are still under study condition, are the use of the compensation cell using the Buck EIE inverter and the cycloconverter with three-phase input and single-phase output. For future works, one can also mention the use of soft switching for the compensation converters and the use of multilevel converters. The main advantage of using multilevel compensation is the fact that the output voltage to be compensated can be divided into several cells, thus reducing the voltage stress of the power switches to a higher compensation level. Also, the multilevel topology is a suitable solution for high power and high voltage applications. On the other hand, more switches are used in this process.

ACKNOWLEDGEMENT

This research was partially financed by National Council for Scientific and Technological Development (CNPq) under Grants 406845/2013-1, 472477/2013-2, 304479/2017-9, 304489/2017-4; the Coordination for the Improvement of Higher Education Personnel (CAPES); the Research Support Foundation of the State of Minas Gerais (FAPEMIG), and the Federal University of Uberlandia (UFU).

AUTHOR'S CONTRIBUTIONS

GUIMARÃES, E.C.: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **FREITAS, P.A.R.:** Data Curation, Investigation, Methodology, Validation, Visualization. **MELO, F.C.:** Investigation, Methodology, Validation, Visualization, Writing – Review & Editing. **LIMA, G.B.:** Investigation, Methodology, Validation, Visualization. **FREITAS, L.C.:** Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Resources, Supervision, Validation, Visualization. **FREITAS, L.C.G.:** Formal Analysis, Funding Acquisition, Investigation, Methodology, Project Administration, Resources, Validation, Visualization, Writing – Review & Editing.

PLAGIARISM POLICY

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BIOGRAPHY

Érico C. Guimarães was born in Uberlândia, Minas Gerais, Brazil, in 1991. He received the B.S. degree in 2013 in Electrical Engineering from the Federal University of Uberlândia (UFU), Brazil, and a master's degree (2016) from the postgraduate program in Electrical Engineering at UFU in Power Electronics, working at the Power Electronics Research Center (NUPEP). During his master's degree he studied and developed control techniques for AC-AC converters. He is currently a PhD student in Electrical Engineering at the same institution. His main topics of interest are: Microgrids, Distributed Generation, Renewable Energy, Control Methods and Power Quality.

Pedro A. R. de Freitas was born in Uberlândia, Minas Gerais, Brazil, in 1990. He received the B.S. and master's degrees in electrical engineering from the Federal University of Uberlândia (UFU), in 2012 and 2014, respectively, where he is currently pursuing the Ph.D. degree in power electronics. In 2014, he joined the Federal Institute of the Triângulo Mineiro, IFTM, where he is also a Professor. His research interests include photovoltaic systems and sustainable energies.

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Gustavo B. Lima was born in Ibiassucê, Brazil, in 1986. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Uberlândia (UFU), Uberlândia, Minas Gerais, Brazil, in 2010, 2012, and 2015, respectively. In 2017, he joined as a Faculty Member of UFU, where he is currently developing teaching and research activities in the area of power electronics and power systems as a member of the Power Electronics Research Center (NUPEP), Faculty of Electrical Engineering, UFU. His research interests include hybrid rectifiers, digital control applied to power electronics, and power factor correction.

Luiz C. Freitas was born in Monte Alegre, Minas Gerais, Brazil, in April 1952. He received the M.Sc. and Ph.D. degrees in power electronics from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1985 and 1992, respectively. In 1991, he founded the Research Center in Power Electronics, Federal University of Uberlândia (UFU). He has authored a variety of papers particularly in the areas of soft switching, DC–DC, DC–AC, and AC–DC converters. He has published in PESC-92, APEC-93, PESC-93, and IEEE Transactions on Power Electronics, in January 1995, a family of soft-switching converters that promote the driving input and output of switches with zero voltage, which, since then, he has been widely used in research related to non-dissipative switching converters. Since 1996, he has been a Researcher recognized by the National Council for Scientific and Technological Development (CNPq) with a Research Productivity Grant. He is currently a retired Professor with UFU, where he is a collaborating Researcher with the Postgraduate Program, Faculty of Electrical Engineering. He has more than 79 articles published in national and international journals, and more than 244 papers published in conferences. His research interests include the design and development of power electronics converters.

Luiz C. G. Freitas was born in Uberlândia, Brazil, in 1976. He received the Graduate degree in electrical engineering with emphasis on power systems and the master's and Ph.D. degrees in electrical engineering with emphasis on power electronics from the Federal University of Uberlândia (UFU), in 2001, 2003, and 2006, respectively. In his doctoral thesis, he developed an innovative topological design of a three-phase hybrid rectifier for high power drive systems. In 2012, he received the Second Prize Paper Award of the IEEE-IAS-Industrial Automation and Control Committee (IACC) for his contribution to the development of hybrid rectifier structures. In 2008, he joined as a Faculty Member of UFU, where he is currently developing teaching and research activities in the area of power electronics and power systems. Since 2010, he has been the Coordinator of the Power Electronics Research Center (NUPEP), Faculty of Electrical Engineering, UFU. Since 2013, he has been a Researcher recognized by the National Council for Scientific and Technological Development (CNPq) with a Research Productivity Grant. His research interests include electrical engineering, conversion and rectification of electric energy, working on various topics related to power electronics, electrical power quality, and renewable energy.