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A Finite Control Set Model Predictive Control Algorithm with Low Complexity for Neutral-Point Clamped Converters with Switching Constraints

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ABSTRACT This paper proposes a Finite Control Set Model Predictive Control algorithm with low complexity for three-phase grid-tied Neutral-Point Clamped converters with switching constraints. The system model is represented in the converter output line-to-line voltage coordinates, where the voltage vectors are integer values. First, the unconstrained solution is obtained to control the converter-side currents. Ellipse constraints are inscribed in the Space Vector diagram to ensure the switching transitions between only adjacent levels in the phase voltages. Moreover, the inverter voltage vector to be implemented in the next sampling period is obtained with low complexity by rounding the constrained voltage vector. Afterward, a cost function is calculated for the redundancies of the chosen inverter voltage vector, aiming to balance the DC-link capacitor voltages. The proposed algorithm presents advantages such as low computation burden, fast transient response, and good steady-state performance. Real-time Hardware-in-the-Loop results are presented to demonstrate the good performance of the proposed algorithm compared to other techniques with a reduced computational burden. Moreover, experimental results show the effectiveness of the proposed algorithm in terms of transient response and steady-state performance.

KEYWORDS Computational burden, Finite Control Set Model Predictive Control, grid-tied converters, Neutral-Point Clamped.

I. INTRODUCTION

Finite Control Set Model Predictive Control (FCS-MPC) has emerged as a competitive alternative for multilevel converters due to its numerous advantages over classical control techniques [1], [2]. These advantages include the integration of system and converter operation constraints, the ability to control multiple variables, and the incorporation of control and modulation within the same algorithm [3]. Recent developments consolidate the application of FCS-MPC algorithms for various classical voltage-fed multilevel converter topologies, such as Neutral-Point Clamped (NPC), Flying Capacitor (FC), Cascaded H-Bridge (CHB), Modular Multilevel Converter (MMC), among others [4]–[7]. The complexity of the FCS-MPC algorithm is typically related to the number of levels in the converter and the prediction horizon [8]. As a result, the computational burden of the FCS-MPC is usually high for multilevel converters with a high number of levels, requiring digital processors with high computational capability for real-time calculations.

Considering the NPC converter, several FCS-MPC algorithms have been recently proposed in the literature [9]–[11]. In this context, the cost function for the MPC algorithm can be designed according to the application of the NPC converter to control different variables, such as the output currents and voltages, balance the voltages of the dc-link capacitors, control the neutral-point current, reduce the common-mode voltages and minimize the switching losses of the semiconductor devices [12]–[14]. Moreover, to minimize the MPC algorithm's computational burden for the NPC converter, a fast MPC was proposed in [15] to find the nearest vector from the optimal voltage reference in $\alpha\beta$ coordinates. Also, in [12], a computationally efficient Direct MPC was proposed for a Back-to-Back NPC converter system for a wind generation plant. The voltage vectors are divided into different regions, and by the appropriate selection of the candidate regions, a reduced number of voltage vectors is considered for the cost function calculations.

Usually, the conventional FCS-MPC algorithms proposed for multilevel converters require a high computational burden for evaluating the cost function online, due to the high number of possible voltage vectors. Therefore, different authors have been working to deal with this issue and some alternatives have been proposed in the literature [16]. In this context, it is possible to mention the division of

the whole optimization problem into smaller ones [17]–[20], the implementation of optimization algorithms, such as the Sphere Decoding Algorithm (SDA) [21], as well as dynamic programming and greedy algorithms, which are also proposed to reduce the computational burden of the FCS-MPC algorithms [22]. Moreover, in [23], a Cascaded FCS-MPC algorithm was proposed, that divides the optimization problem into two cascaded FCS-MPC problems. First, a cost function composed of a current tracking error term is considered. Afterward, a second cost function is evaluated for the redundancies of the voltage vector selected in the first stage. As a result, this approach avoids the need to design weighting factors for the cost function. Also, in [24], a simplified branch-and-bound algorithm is proposed for CHB converters to reduce the number of calculations of the FCS-MPC algorithm. In both cases, the computational burden depends on the number of voltage levels of the converter, and the execution time still increases when the number of converter voltage levels increases. Another alternative is minimizing the number of calculations for the cost function by reducing the set of candidate voltage vectors for each sampling period [25], [26].

In order to reduce the computational burden for digital implementation, this paper presents a low-complexity FCS-MPC algorithm for NPC converters with switching constraints and is an extension of the paper presented in [27]. The system model of the NPC converter connected to the grid by an LCL filter is represented in the converter output line-to-line voltage coordinates, where the converter voltage vectors have only integer entries. The unconstrained voltage reference to control the converter output currents is projected in the space vector diagram, which is also represented in the converter line-to-line voltage coordinates [28]. In addition, constraints of adjacent phase-voltage level transitions and feasibility are included in the Space Vector (SV) diagram, limiting the search space to a two-level SV diagram around the last implemented voltage vector. In each sampling period, first, the inverter voltage vector to be implemented is obtained by rounding the constrained reference, without the need for multiple cost function evaluations and weighing factors design. Then, the set of redundant phase-voltage vectors is defined based on common-mode voltage limitation criteria, and the redundancies with transitions only between adjacent phase voltage levels are considered by a cost function to balance the DC-link capacitor voltages. The proposed FCS-MPC algorithm presents advantages such as a low computational burden, fast transient response, and good steady-state performance. Moreover, it can be easily expanded to other multilevel topologies without loss of generality. The main contributions of this paper are:

- an improved literature review compared to [27];
- a detailed description of the proposed method with new analyses of each step of the algorithm;
- inclusion of the converter switching constraints as ellipses in the space vector diagram;
- experimental validation to demonstrate the good performance of the proposed algorithm;
- lower computational burden compared to the methods proposed in [22] and in [23].

The rest of the paper is divided as follows: Section II presents the system model of the grid-tied NPC converter in the line-to-line voltage coordinates; Section III describes the proposed FCS-MPC algorithm with the inverter constraints and control of the neutral-point current; Section IV presents Hardware-in-the-Loop (HIL) comparative results, and the experimental results of the proposed algorithm are shown in Section V. Finally, the main conclusions of this paper are summarized in Section VI.

II. SYSTEM MODEL

The system model of the proposed FCS-MPC is described in this section. Figure 1 presents the three-phase NPC converter connected to the grid by an LCL filter and Table 1 presents the switching states of the NPC converter.

A. Operation of the NPC Inverter

Compared to the two-level converter, the NPC converter presents advantages such as output voltages with a higher number of levels and reduced Total Harmonic Distortion (THD), lower reverse blocking voltages across the semiconductor devices for the same DC-link voltage. These advantages make the NPC converter suitable for power conversion applications, including renewable energy systems, electric vehicles, and industrial motor drives [29], [30].

The NPC converter presents a unique switching state combination for each output voltage level and there are no redundant switching states for each phase voltage level. On the other hand, some line-to-line voltage levels can be synthesized by different phase-voltage combinations of switching states, which are called redundancies. In the NPC converter, each redundancy can result in different current polarities in the neutral point of the DC link. Usually, under normal operation conditions, the blocking voltages across the NPC semiconductor switches are clamped to half the value of the DC-link voltage. However, due to some non-idealities, such as dead-time, parasitic capacitances, and inductances, the internal switches (S_{2x} and S_{3x}) can be submitted to the total DC-link voltage [31]. To prevent this over-voltage across the semiconductor devices S_{2x} and S_{3x} and ensure the safe operation of the NPC converter, the transition between states "-1" to "1", and vice-versa, should be avoided [32].

B. Simplified System Model

In this paper, the LCL filter is approximated by an L filter and the filter capacitor voltages are considered as the disturbances [33]. As a result, only the inverter-side currents and filter capacitor voltages need to be measured, reducing the number of sensors in the system. Moreover, resistors are included in series with the filter capacitors to reduce the effects of the LCL filter resonance.

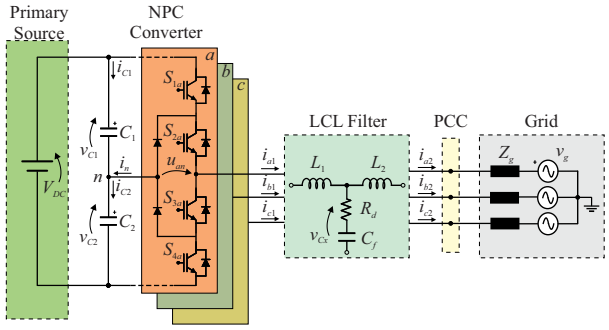


FIGURE 1. Three-phase grid-tied NPC converter with LCL filter [27].

TABLE 1. Phase Switching States of the NPC inverter.

State	S_{1x}	S_{2x}	S_{3x}	S_{4x}	Phase Voltage (u_{xn})
1	ON	ON	OFF	OFF	$V_{DC}/2$
0	OFF	ON	ON	OFF	0
-1	OFF	OFF	ON	ON	$-V_{DC}/2$

By applying Kirchoff's Voltage Law (KVL) in the inverter-side of the LCL filter, it is possible to write the system equations [27], [28]:

$$\begin{aligned} -u_{an} + L_1\frac{di_{a1}}{dt} + v_{Ca} - v_{Cb} - L_1\frac{di_{b1}}{dt} + u_{bn} = 0, \\ -u_{bn} + L_1\frac{di_{b1}}{dt} + v_{Cb} - v_{Cc} - L_1\frac{di_{c1}}{dt} + u_{cn} = 0, \end{aligned} \tag{1}$$

where u_{an}, u_{bn} and u_{cn} represent the NPC output phase-voltages, v_{Ca}, v_{Cb} and v_{Cc} are the LCL filter capacitor voltages, i_{a1}, i_{b1} and i_{c1} are the converter-side currents and L_1 is the converter-side filter inductance. Given that the voltage vectors of a three-leg converter are always located in a plane, a two-dimensional coordinate system can be chosen to represent them [34], [35]. From (1), the dynamic equations of the system can be represented in the output line-to-line coordinates, resulting in:

$$\begin{aligned} L_1\frac{d}{dt}\left(i_{ab1}\right) = -v_{Cab} + u_{ab}, \\ L_1\frac{d}{dt}\left(i_{bc1}\right) = -v_{Cbc} + u_{bc}, \end{aligned} \tag{2}$$

where i_{ab1} and i_{bc1} can be interpreted as the converter-side line-to-line currents, v_{Cab} and v_{Cbc} are the line-to-line filter capacitor voltages and u_{ab} and u_{bc} are the line-to-line converter output voltages. In this paper, the "ca" currents are omitted, once they are linearly dependent on "ab" and "bc". Figure 2 shows the SV diagram for the three-phase NPC inverter, which is represented in the output line-to-line voltages coordinate system and normalized to half the value of the dc-link voltage, where the voltage vectors assume only integer values [28].

To obtain the discrete-time system equations, a fixed small sampling period T_s is assumed, and the Euler discretization

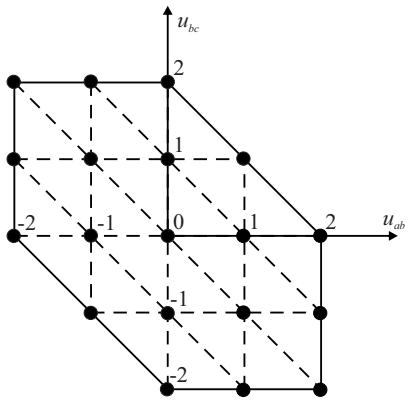


FIGURE 2. Normalized SV diagram for a three-phase NPC inverter in the output line-to-line voltages coordinate system [28].

method is applied to (2), which results in:

$$\begin{aligned} i_{ab1(k+1)} = i_{ab1(k)} + \frac{T_s}{L_1}u_{ab(k)} - \frac{T_s}{L_1}v_{Cab(k)}, \\ i_{bc1(k+1)} = i_{bc1(k)} + \frac{T_s}{L_1}u_{bc(k)} - \frac{T_s}{L_1}v_{Cbc(k)}, \end{aligned} \tag{3}$$

which are also represented in the output line-to-line voltage coordinate system.

III. PROPOSED FCS-MPC ALGORITHM

This section presents the proposed FCS-MPC, whose block diagram is shown in Figure 3. In this paper, it is considered that the inverter-side currents $\mathbf{i}_1 = [\ i_{ab1} \quad i_{bc1}\ ]^T$ will properly track their references $\mathbf{i}_1^* = [\ i_{ab1}^* \quad i_{bc1}^*\ ]^T$ for each sampling period, such as [36]:

$$\begin{aligned} i_{ab1(k+2)} = & i_{ab1(k+2)}^*, \\ i_{bc1(k+2)} = & i_{bc1(k+2)}^*, \end{aligned} \tag{4}$$

where the sampling period $k+2$ considers the time delay for digital implementation on the microprocessor. The references for the converter-side currents (i_1^*) can obtained from the grid-side currents references (i_2^*), in the stationary reference frame $\alpha\beta$, by compensating the reactive power of the LCL filter capacitor, as [33]:

$$\begin{bmatrix} i_{1\alpha}^* \\ i_{1\beta}^* \end{bmatrix} = \begin{bmatrix} i_{2\alpha}^* \\ i_{2\beta}^* \end{bmatrix} + \omega\, C_f \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} v_{C\alpha} \\ v_{C\beta} \end{bmatrix}. \tag{5}$$

By substituting (4) in (3) and considering the implementation delay, the inverter unconstrained output voltage references to achieve the current references in the next sampling period can be determined as:

$$\begin{aligned} u_{ab(k+1)}^* = \frac{L_1}{T_s}\left(i_{ab1(k+2)}^* - i_{ab1(k+1)}\right) + v_{Cab(k+1)}, \\ u_{bc(k+1)}^* = \frac{L_1}{T_s}\left(i_{bc1(k+2)}^* - i_{bc1(k+1)}\right) + v_{Cbc(k+1)}, \end{aligned} \tag{6}$$

where the unconstrained line-to-line reference voltage vector is defined as $\mathbf{u}_{(k+1)}^* = [\ u_{ab(k+1)}^* \quad u_{bc(k+1)}^*\ ]^T$.

Note that the current references in the stationary reference frame ($\alpha\beta$) for $k+2$ can be estimated from the values of

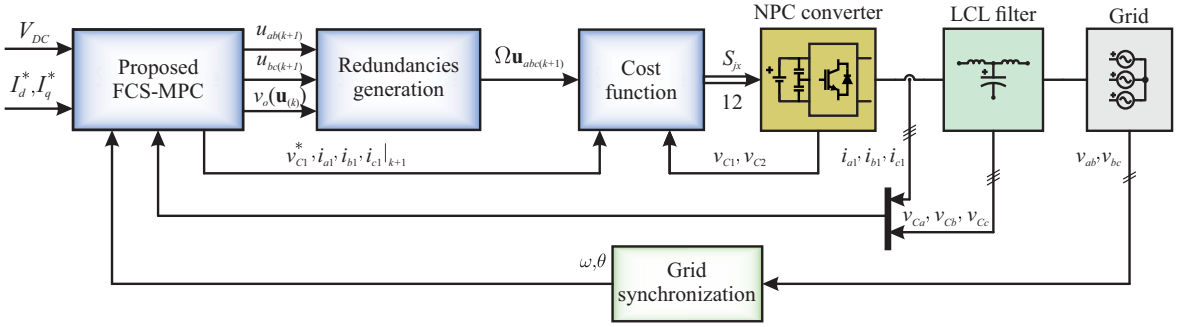


FIGURE 3. Block diagram of the proposed FCS-MPC algorithm.

the current references for k, considering the fundamental component, as:

$$\begin{bmatrix} i^*_{1\alpha(k+2)} \\ i^*_{1\beta(k+2)} \end{bmatrix} = \begin{bmatrix} \cos(2\omega T_s) & -\sin(2\omega T_s) \\ \sin(2\omega T_s) & \cos(2\omega T_s) \end{bmatrix} \begin{bmatrix} i^*_{1\alpha(k)} \\ i^*_{1\beta(k)} \end{bmatrix}, \tag{7}$$

where the references in the inverter output line-to-line voltage system are obtained from a coordinate transformation.

A. Switching Constraints

In this paper, the unconstrained reference vector $\mathbf{u}^*_{(k+1)}$ is limited to guarantee its feasibility and the proper voltage clamping of the NPC inverter. First, the unconstrained reference vector is constrained to a region where the candidate switching vectors have at least one redundancy that switches at most one level in each phase voltage from the last implemented vector. So, the voltage clamping of the internal switches of the NPC legs is ensured. Then, the reference voltage vector is constrained to result in a region where only feasible inverter voltage vectors can be selected from it.

To simplify the implementation of the constraints, ellipses are considered to limit the region for the reference voltage vector in the SV diagram, as illustrated in Figure 5. The quadratic equation of the ellipse is given by:

$$u_{ab}^2 + u_{ab}u_{bc} + u_{bc}^2 = c. \tag{8}$$

Initially, a coordinate translation is carried out, where the last implemented line-to-line voltage vector $\mathbf{u}_{(k)} = [\ u_{ab(k)} \quad u_{bc(k)}\ ]^T$ is set as the origin of a new line-to-line coordinate system, such as:

$$\begin{aligned} u^{*\prime}_{ab(k+1)} &= u^{*}_{ab(k+1)} - u_{ab(k)}, \\ u^{*\prime}_{bc(k+1)} &= u^{*}_{bc(k+1)} - u_{bc(k)}. \end{aligned} \tag{9}$$

Then, the unconstrained vector in the new coordinates $\mathbf{u}^{*\prime}_{(k+1)} = [\ u^{*\prime}_{ab(k+1)} \quad u^{*\prime}_{bc(k+1)}\ ]^T$ is tested by the first ellipse constraint, which limits the convex hull of the candidate vectors and can be done by substituting (9) in (8), resulting in:

$$u^{*\prime 2}_{ab(k+1)} + u^{*\prime}_{ab(k+1)}u^{*\prime}_{bc(k+1)} + u^{*\prime 2}_{bc(k+1)} = c_{1(k+1)}, \tag{10}$$

where $c_{1(k+1)}$ is the calculated size of the ellipse for the unconstrained vector in the new coordinates and is computed at every sampling instant for a given voltage reference.

If $c_{1(k+1)}$ is larger than F_1, which defines the maximum size of the ellipse where the set of candidate voltage vectors meet the first constraint, then the reference vector is limited as:

$$\begin{aligned} u^{*\prime}_{ab(k+1)} &= u^{*\prime}_{ab(k+1)}\sqrt{\frac{F_1}{c_{1(k+1)}}} \\ u^{*\prime}_{bc(k+1)} &= u^{*\prime}_{bc(k+1)}\sqrt{\frac{F_1}{c_{1(k+1)}}}, \end{aligned} \tag{11}$$

where $F_1 = \frac{3}{16}V_{dc}^2$ is the maximum size of the ellipse of the switching constraint, represented by the blue curve in Figure 5. As a result, the limited SV space corresponds to a two-level SV diagram around $\mathbf{u}(k)$, as illustrated in Figure 5, where at least one redundancy of each voltage vector meets the switching transitions constraint.

Then, the constrained reference vector is remapped to the original line-to-line coordinate system (u_{ab}, u_{bc}), where the second constraint is evaluated to guarantee that the reference vector lies inside the maximum feasible region, as represented by the red ellipse in Figure 5. The second constraint is computed by:

$$u^{*2}_{ab(k+1)} + u^{*2}_{ab(k+1)}u^{*2}_{bc(k+1)} + u^{*2}_{bc(k+1)} = c_{2(k+1)}, \tag{12}$$

where $c_{2(k+1)}$ is the calculated size of the ellipse in the original coordinate system for a given reference voltage vector.

If $c_{2(k+1)}$ is larger than the maximum ellipse length for the feasible vectors F_2, the reference vector is limited over it, as:

$$\begin{aligned} u^{*}_{ab(k+1)} &= u^{*}_{ab(k+1)}\sqrt{\frac{F_2}{c_{2(k+1)}}}, \\ u^{*}_{bc(k+1)} &= u^{*}_{bc(k+1)}\sqrt{\frac{F_2}{c_{2(k+1)}}}, \end{aligned} \tag{13}$$

where $F_2 = \frac{13}{16}V_{dc}^2$ is the maximum size of the ellipse of the feasible constraint, represented by the red curve in Figure 5. Note that the maximum size of each ellipse can be obtained by substituting the coordinates of any vector that lies over it, in (8).

A low complexity way to obtain the solution voltage vector to be implemented is by rounding the reference vector

such as:

$$\begin{bmatrix} u_{ab(k+1)} \\ u_{bc(k+1)} \end{bmatrix} = \text{round} \begin{bmatrix} u^*_{ab(k+1)} \\ u^*_{bc(k+1)} \end{bmatrix}. \quad (14)$$

In this paper, by introducing the ellipse constraints, the selected voltage vector, in the line-to-line voltage coordinates, presents at least one redundancy that has at most one phase-voltage level transition from the last implemented voltage vector. However, it can be noted that with the projection of the unconstrained solution over the ellipse constraints, the chosen vector may result in a sub-optimal solution, according to the operational point of the system [27]. On the other hand, the cost function difference between the sub-optimal and the optimal solution is small, resulting in a negligible impact on the grid-side currents tracking error.

In the SV diagram presented in Figure 2, some vectors have more than one combination of switching states which result in the same line-to-line voltages. To select a specific redundant vector in the phase-voltage space, a common-mode voltage criterion is used to generate the set of redundancies that present at most a single phase voltage level transition from the last implemented vector. It is based on the common-mode voltage difference Δv_o from the last implemented vector $\mathbf{u}_{(k)}$ to the candidate redundancies of the selected vector $\mathbf{u}^*_{(k+1)}$, such as:

$$\Delta v_o = v_o(\mathbf{u}_{(k)}) - v_o(\mathbf{u}^*_{(k+1)}), \quad (15)$$

where $v_o(\mathbf{u}_{(k)})$ is the common-mode voltage of the last implemented vector and $v_o(\mathbf{u}^*_{(k+1)})$ refers to the common-mode voltage of the candidate redundancy.

Considering an SV diagram of a two-level three-phase inverter, where each phase voltage switches at most one level, the common mode voltage difference of two different voltage vectors is always less or equal to 2, i.e, $|\Delta v_o| \leq 2$. By expanding this criterion to the three-level SV diagram presented in Figure 2, the redundancies that satisfy it are selected as the set of candidate vectors $\Omega\mathbf{u}_{abc(k+1)}$ to be implemented in the next sampling period. On the other hand, the redundancies that present more than one switching transition in each phase from the last implemented vector are not included in the set of candidate vectors and can not be implemented in the next sampling period.

B. Cost Function for Neutral-Point Balance

From the set of redundant vectors, a cost function is evaluated to balance the DC-link voltage of the NPC converter. The cost function is composed of the capacitor voltage error, such as:

$$J = \left(\frac{V_{dc}}{2} - v_{c1(k+2)} \right)^2, \quad (16)$$

where $v_{c1(k+2)}$ corresponds to the predicted voltage over the upper DC link capacitor C_1 at sampling instant $(k+2)$, which can be estimated by:

$$v_{c1(k+2)} = v_{c1(k+1)} + \frac{T_s}{C_1} i_{c1(k+1)}, \quad (17)$$

where $i_{c1(k+1)}$ is the predicted current that will flow through C_1. It can be estimated from the equation of the current that flows into the neutral point, that is:

$$i_{n(k+1)} = -\sum_x i_{x1(k+1)} \left(1 - 2 \left| \frac{u_{xn(k+1)}}{V_{dc}} \right| \right), \quad (18)$$

where $x \in \{a, b, c\}$ indicates the corresponding inverter phase and $2\frac{u_{xn}}{V_{dc}} \in \{-1, 0, 1\}$ is the candidate inverter phase voltage to be implemented.

Given that the total DC link voltage is constant or varies slowly in time, we can assume that:

$$\frac{dV_{dc}}{dt} \approx 0, \quad (19)$$

we can write:

$$i_{c1} + i_{c2} = 0. \quad (20)$$

Now, from Kirchoff's Current Law (KCL) on the dc link mid-point node, as seen in Figure 1, we have:

$$i_{c1} + i_n = i_{c2}, \quad (21)$$

where the simultaneous solution of (20) and (21) results in:

$$i_{c1} = -\frac{1}{2} i_n. \quad (22)$$

Assuming that the total dc-link voltage is constant or varies slowly in time, as (21), we have:

$$i_{c1(k+1)} = \sum_x i_{x1(k+1)} \left(\frac{1}{2} - \left| \frac{u_{xn(k+1)}}{V_{dc}} \right| \right). \quad (23)$$

Since we are addressing a three-phase three-wire system, (23) can be simplified to:

$$i_{c1(k+1)} = -\sum_x i_{x1(k+1)} \left| \frac{u_{xn(k+1)}}{V_{dc}} \right|. \quad (24)$$

As a result, it is possible to obtain the feasible converter phase voltage vectors by mapping the constrained solution line-to-line voltage vector into the converter phase voltage space. For the NPC converter, one, two, or three inverter phase voltage vectors can be obtained for each line-to-line voltage vector, $\frac{2}{V_{dc}} \begin{bmatrix} u_{an} & u_{bn} & u_{cn} \end{bmatrix}^T$. In the cases where two or three redundancies satisfy the common-mode voltage difference (15), the cost function (16) is evaluated and the redundancy with the lowest cost function is implemented during the sampling period from $(k+1)$ to $(k+2)$. Figure 4 illustrates the flowchart of the proposed algorithm.

C. Numerical Example

Figure 5 shows an example of how the proposed algorithm works. Let us consider that, for a given sampling instant, the last implemented vector $\mathbf{u}_{(k)}$ was $u_{ab(k)} = 2$ and $u_{bc(k)} = -1$, normalized by half the DC-link voltage, as represented by the yellow dot in Figure 5. This vector has the phase-voltage coordinates as $\mathbf{u}_{abc(k)} = \begin{bmatrix} 1 & -1 & 0 \end{bmatrix}^T$, which has $v_o(\mathbf{u}_{(k)}) = 0$. Given the normalized unconstrained reference $\mathbf{u}^*_{(k+1)} = \begin{bmatrix} 3.3 & -0.2 \end{bmatrix}^T$, illustrated by the first blue dot in Figure 5, the coordinate transformation results in $\mathbf{u}^{*\prime}_{(k+1)} = \begin{bmatrix} 1.3 & 0.8 \end{bmatrix}^T$. Calculating the ellipse equation

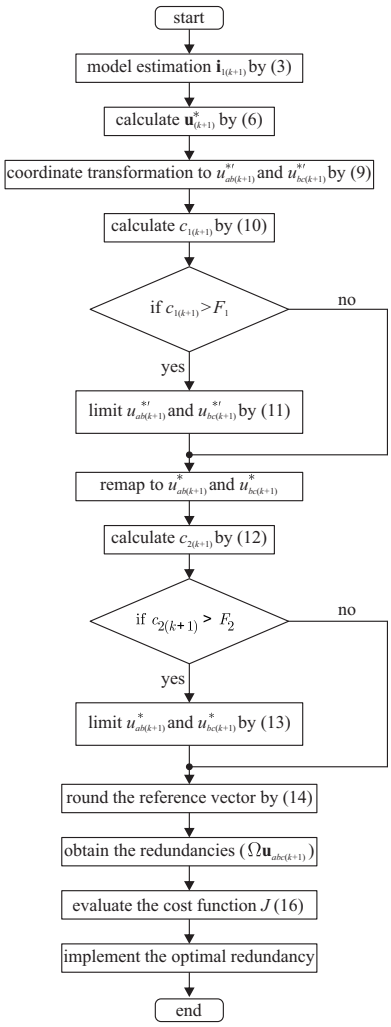


FIGURE 4. Flowchart of the proposed FCS-MPC algorithm.

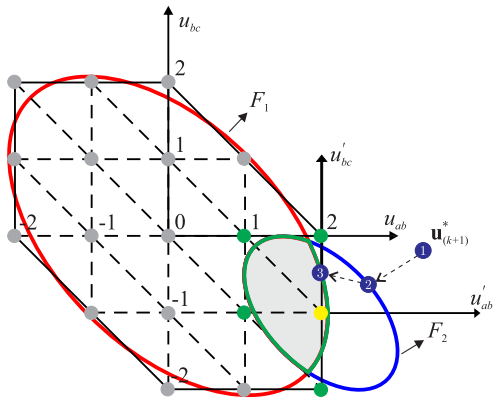


FIGURE 5. Normalized SV diagram with ellipse constraints and its resultant limited region.

for this vector results in $c_{1(k+1)} = 3.37$, while $F_1 = 0.75$. As $c_{1(k+1)} > F_1$, it is necessary to limit the reference vector over the blue ellipse using (11), which results in $\mathbf{u}^{*\prime}_{(k+1)} = \begin{bmatrix} 0.613 & 0.377 \end{bmatrix}^T$. Now, by remapping this constrained vector to the line-to-line voltages coordinate system, it results in $\mathbf{u}^{*}_{(k+1)} = \begin{bmatrix} 2.613 & -0.633 \end{bmatrix}^T$, as indicated by the second blue dot in Figure 5. The second constraint is then calculated by (12) and results in $c_{2(k+1)} = 5.5744$, with $F_2 = 3.25$, which indicates that the reference vector is outside the feasibility region of the SV diagram. Then, the reference vector should be limited over the red ellipse, resulting in $\mathbf{u}^{*}_{(k+1)} = \begin{bmatrix} 1.99 & -0.48 \end{bmatrix}^T$, represented by the third blue dot in Figure 5. Finally, the nearest vector is found by rounding the constrained reference vector, as (14), which results in $\mathbf{u}_{(k+1)} = \begin{bmatrix} 2 & 0 \end{bmatrix}^T$. Given that the selected vector does not present any redundancy, the phase coordinates vector for the next sampling is equal to $\mathbf{u}_{abc(k+1)} = \begin{bmatrix} 1 & -1 & -1 \end{bmatrix}^T$.

As a second example, let us assume that the resultant vector from rounding a given constrained vector is $\mathbf{u}_{(k+1)} = \begin{bmatrix} 1 & 0 \end{bmatrix}^T$, with the redundancies $\begin{bmatrix} 1 & 0 & 0 \end{bmatrix}^T$ and $\begin{bmatrix} 0 & -1 & -1 \end{bmatrix}^T$, and their common mode voltages 1 and -2, respectively. From (15), the common-mode voltage difference from the last implemented vector, $\mathbf{u}_{(k)} = \begin{bmatrix} 2 & -1 \end{bmatrix}^T$, are -1 and 2, respectively, indicating that both redundancies present at most one voltage transition in the phase-voltages from the last implemented vector, and are included in the set of candidate vectors ($\Omega\mathbf{u}_{abc(k+1)}$). From the first redundancy, a current equal to $i_{a(k+1)}$ will flow into the neutral point while the second redundancy imposes a neutral-point current equal to $-i_{a(k+1)}$. For each case, (23) is calculated and the capacitor voltage $v_{c1(k+2)}$ is predicted. Aiming to bring the capacitor voltages close to their reference values, the cost function J is calculated for both redundancies, and the one with the lowest cost is implemented during the next sampling period.

Note that the cost function is computed at most two times for the NPC inverter, once the null vector does not affect the current at the neutral point. In addition, by the common-mode voltage criteria, the redundant state of the null vector which presents the minimum number of commutations from the last implemented vector, i.e., the lowest Δv_o, is automatically selected for the next sampling period. Compared to the classical FCS-MPC, where the cost function is computed for the 27 different converter switching states, the computational burden is significantly reduced, making it faster to compute by commercial microprocessors.

IV. HARDWARE-IN-THE-LOOP RESULTS

In this section, the performance of the proposed FCS-MPC algorithm is presented and compared to other FCS-MPC algorithms to highlight the advantages of the proposed technique. To do that, real-time Hardware-in-the-Loop results are obtained by Typhoon HIL model 404, and the algorithms are implemented in a Digital Signal Processor (DSP), model TMS320F28377D, from Texas Instruments, as demonstrated in Figure 6. In addition, the main system parameters are presented in Table 2.

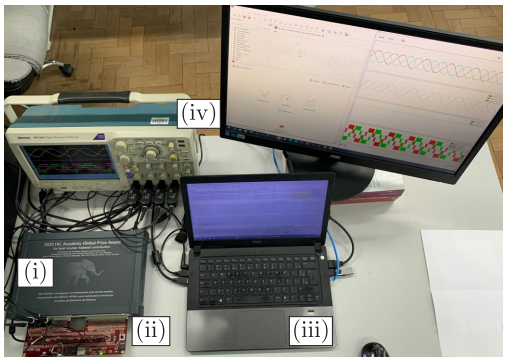


FIGURE 6. Typhoon HIL 404 and test-bed for real-time results. (i) HIL device, (ii) DSP interface board, (iii) computer, and (iv) oscilloscope.

TABLE 2. System parameters of the grid-tied NPC with LCL filter for HIL and experimental results.

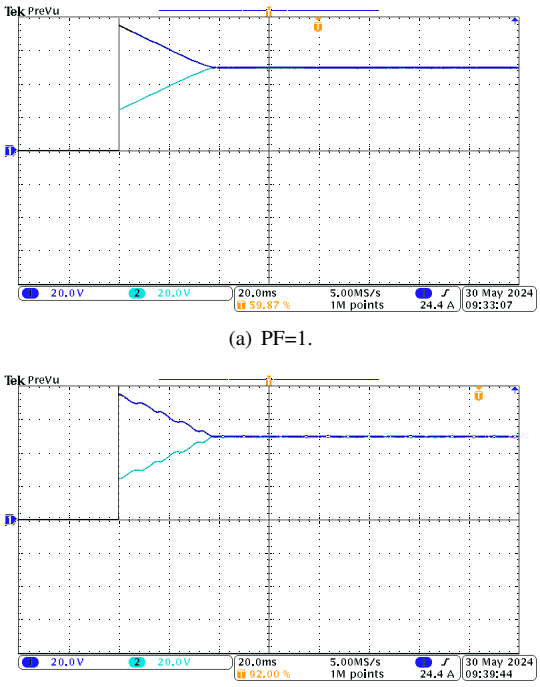
Parameter	Symbol	Value
Grid voltage	v_g	40/70 V
Grid Frequency	f	60 Hz
Grid impedance	Z_g	5 μH, 0.1 $m\Omega$
DC-link voltage	V_{DC}	100 V
DC-link capacitors	C_1, C_2	4700 μF
Inverter-side filter inductance	L_1	900 μH
LCL filter capacitance	C_f	100 μF
Damping resistance	R_d	1 Ω
Grid-side filter inductance	L_2	100 μH
Sampling frequency	f_s	40 kHz

Initially, the DC-link capacitor voltage balance is analyzed for two different power factors (PF). In this case, an unbalanced DC link is considered for PF=1, as presented in Fig. 7(a), and PF=0.7, such as in Fig. 7(b). As can be seen, when the test starts, the DC-link capacitor voltages of the NPC converter are quickly balanced to their reference value, indicating the effectiveness of the cost function adopted in the proposed algorithm. Although high-frequency ripple appears in the capacitor voltages for PF=0.7, they remain balanced to their reference values with similar capacitor voltages offset (vcf) as in the case where PF=1, which are 0.29% and 0.17%, respectively. The vcf is computed as:

$$vcf(\%) = 100\frac{|V_{cc}/2 - \bar{v}_{c1}|}{V_{cc}/2}, \tag{25}$$

where $\bar{v}_{c1}$ is the measured mean value of C_1.

To compare the performance of the proposed FCS-MPC with similar low complexity approaches, a Branch and Bound FCS-MPC [22] and a Cascaded FCS-MPC [23] algorithms were implemented in the HIL device for the same system and parameters. The Branch and Bound FCS-MPC algorithm was proposed to reduce the computational burden of the classical FCS-MPC algorithms. In this approach, the optimization problem is reduced to a two-variable integer quadratic programming problem, where the global optimal solution is evaluated from an algorithm with reduced computational burden. On the other hand, the Cascaded FCS-MPC is based on the division into two cost functions, which are evaluated to, first, find the optimal vector that reduces the current tracking error and, second, obtain the redundancy to control the neutral point current. In this case, compared to the classical FCS-MPC algorithm for an NPC converter, the computational burden is reduced by minimizing the number of calculations of the cost function from 27 to 19 times.



(a) PF=1.

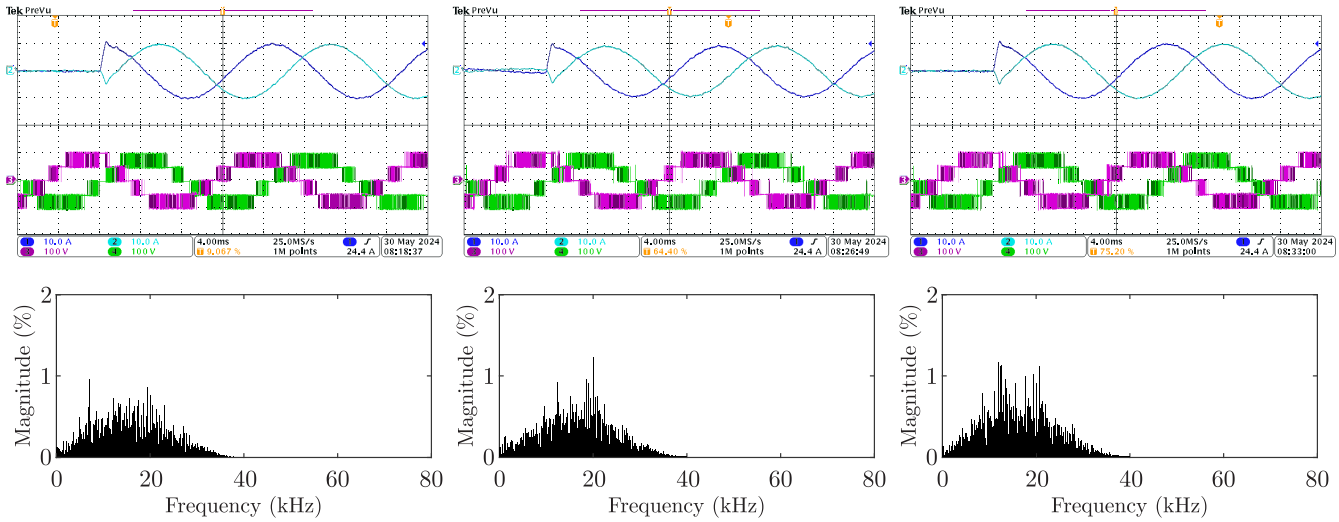
(b) PF=0.7.

FIGURE 7. Dc-link capacitor voltages balance. Horizontal scale: 20 ms/div.. Vertical: 20 V/div..

In order to compare the dynamic response of the three algorithms, Figure 8 presents two grid-side currents and two inverter output line-to-line voltages for a step change in the current reference from 0 to 10A. As illustrated, it is possible to note the similarity of the three algorithms in terms of dynamic performance, where a fast transient response is obtained in all cases. In addition, the Fast Fourier Transform (FFT) of the PWM voltages is presented, indicating an equivalent harmonic spectrum for all algorithms. As illustrated, the main harmonic content is spread around 20 kHz, and the proposed Fast FCS-MPC algorithm presents the lowest THD compared to the other FCS-MPC strategies. Moreover, a steady-state comparison is presented in Table 3 in terms of computational burden, vcf, grid-side current THD, and current Root-Mean-Square Error (RMSE), settling time, and PWM voltages THD. Here, the RMSE is calculated by:

$$\text{RMSE} = \sqrt{\left(\frac{1}{n_s}\sum_{k=0}^{n_s}\left(i_2^*(k) - i_2(k)\right)^2\right)}, \tag{26}$$

where n_s is the number of samples in one cycle, i_2^* is the current reference, and i_2 means the measured current.



(a) Proposed FCS-MPC. (b) Cascaded FCS-MPC [23]. (c) Branch and Bound FCS-MPC [22].

FIGURE 8. Grid currents, converter output line-to-line PWM voltages and their FFT spectra of similar FCS-MPC algorithms. Horizontal scale: 4 ms/div.. Vertical: 100 V/div. and 10 A/div..

TABLE 3. Performance comparison of similar FCS-MPC algorithms.

FCS-MPC Algorithm	Execution Time (μs)	Current THD (%)	Current RMSE (A)	Settling time (ms)	Capacitor voltage offset (%)	PWM Voltage THD (%)
Proposed	3.3	2.15	0.15	50	0.29	36.05
Cascaded [23]	17.0	1.95	0.14	70	0.31	37.79
Branch and Bound [24]	7.4	2.43	0.52	120	0.32	37.52

As presented in Table 3, the proposed FCS-MPC algorithm significantly reduces the computational burden once the inverter voltage vector can be chosen directly by rounding the constrained voltage reference. On the other hand, the cost function needs to be evaluated 19 times for the Cascaded and 5 times for the Branch and Bound algorithm, where complex equations must be determined to find the optimal vector. Moreover, the three FCS-MPC algorithms present similar performances in terms of current THD, RMSE, and capacitor voltage offset. In addition, a similar performance can be also observed in terms of settling time and THD of the PWM voltages. As a result, compared to these techniques, the proposed FCS-MPC algorithm presents the advantages of lower computational burden, switching transitions between only adjacent phase-voltage levels, and has a similar performance compared to optimal algorithms, such as the Cascaded and Branch and Bound FCS-MPC approaches.

V. EXPERIMENTAL RESULTS

To demonstrate the good performance of the proposed FCS-MPC algorithm, experimental results are provided for an NPC inverter connected to the grid by an LCL filter. To do this, an experimental reduced-scale prototype was developed,

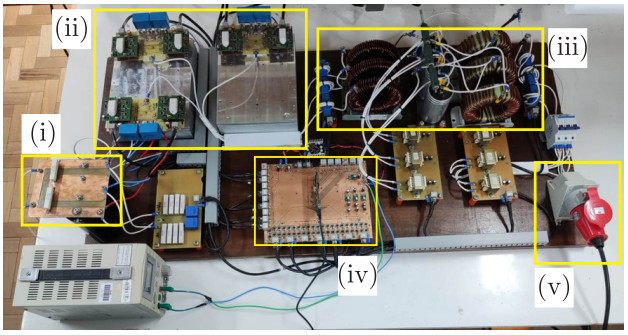
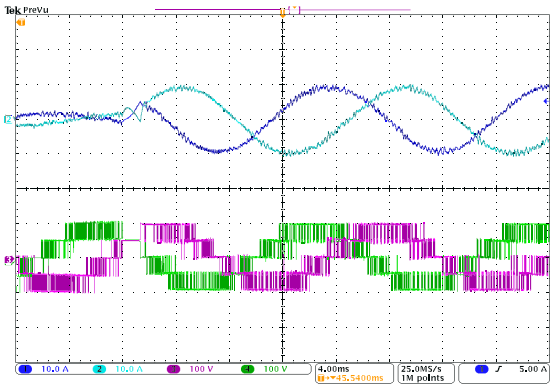


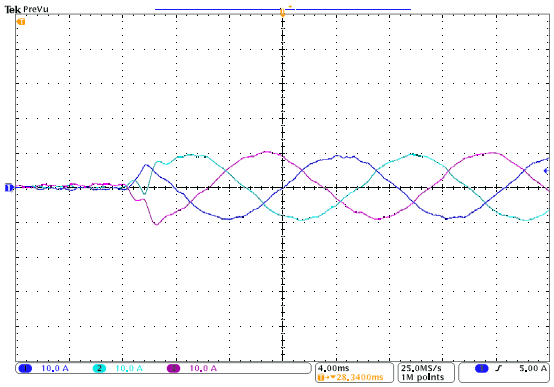
FIGURE 9. Experimental prototype. (i) DC bus, (ii) NPC inverter, (iii) LCL filter, (iv) DSP board, (v) grid connection.

with the same system parameters of the LCL filter presented in Table 2. In the experimental setup, each phase of the NPC converter is implemented by the SK75MLI066T IGBT module, and the gate signals are obtained from the SKYPER 32 PRO drivers, both from SEMIKRON. The experimental setup is shown in Figure 9.

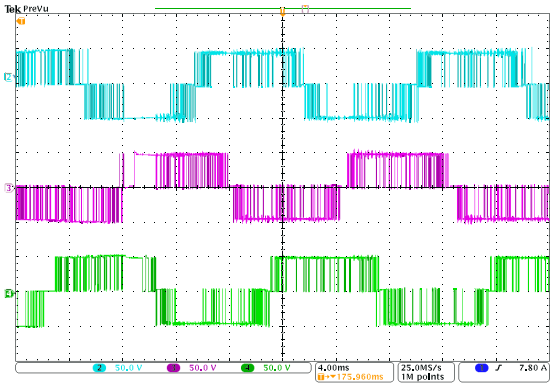
First, experimental results are presented for a step change in the current reference of the proposed FCS-MPC algorithm. Figure 10(a) shows the converter-side currents and Figure



(a) Inverter-side currents and line-to-line voltages.



(b) Grid-side currents.



(c) Inverter phase-voltages.

FIGURE 10. Transient response due to a step change in the current reference. Horizontal: 4 ms/div. Vertical: 10 A/div., 100 V/div., and 50V/div.

10(b) illustrates the line-to-line voltages, and the grid-side currents for a change in the current reference, from 0 to 10 A. As a result, a fast transient response is obtained with reduced steady-state tracking error, indicating the similarity with the results illustrated in Section IV. In addition, Figure 10(c) presents the phase voltages of the NPC inverter for the transient event previously considered. As demonstrated, the phase voltages present switching transitions only between adjacent levels, as expected by the switching constraint implemented in the proposed FCS-MPC algorithm.

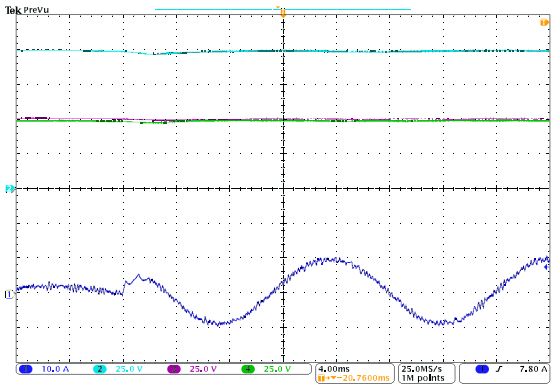


FIGURE 11. DC bus and capacitor voltages and inverter-side current during a transient due to a step change in the current reference. Horizontal: 4 ms/div. Vertical: 10 A/div. and 25 V/div.

Moreover, Figure 11 presents the DC bus and the capacitor voltages, and one inverter-side current at the transient event. It is possible to see that the capacitor voltages remain balanced at their reference value, indicating the effectiveness of the cost function utilized to select the redundancy that minimizes the voltage deviation and to control the DC bus capacitor voltages of the proposed FCS-MPC algorithm.

VI. CONCLUSIONS

This paper presented an FCS-MPC algorithm with a low computational burden for NPC converter with switching constraints. The system model is formulated in the converter output line-to-line voltages, where integer coordinates represent the voltage vectors. In the resultant SV diagram, feasibility and the converter switching constraints are introduced, and the selected voltage vector to be implemented in the next sampling period is found by rounding the constrained reference. From the selected voltage vector, the set of redundancies is obtained from a common-mode voltage constraint criteria, ensuring that the converter switches between only adjacent phase voltage levels, which reduces the *dv/dt* of the output voltages. In addition, a cost function is evaluated for the set of redundant vectors to balance the DC-link capacitor voltages. As a result, the cost function is evaluated at most two times, reducing the computational burden of the algorithm, which is verified by the measurement of the DSP execution time. Although the proposed algorithm can implement a sub-optimal solution in some sampling periods, real-time comparison results indicate a similar performance with optimal FCS-MPC algorithms regarding grid currents, THD, and tracking error, settling time, PWM voltages THD, and capacitor voltage offset. Finally, experimental results for the NPC inverter are provided and illustrate the fast transient response and good performance of the proposed FCS-MPC algorithm, preserving the DC-link voltage balance and the switching constraints of the converter.

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AUTHOR'S CONTRIBUTIONS

SCHUETZ, D.A.: Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Project Administration, Resources, Software, Validation, Writing – Original Draft. **CARNIELUTTI, F.M.**: Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Resources, Supervision, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **ALY, M**: Visualization, Writing – Review & Editing. **NORAMBUENA, M.**: Funding Acquisition, Visualization, Writing – Review & Editing. **RODRIGUEZ, J.**: Funding Acquisition, Validation, Visualization, Writing – Review & Editing. **PINHEIRO, H.**: Conceptualization, Formal Analysis, Funding Acquisition, Investigation, Methodology, Resources, Supervision, Validation, Writing – Review & Editing.

PLAGIARISM POLICY

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