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Bidirectional Switched Capacitor DC-DC Converter Based on Three Level Connection

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ABSTRACT In this paper a pure bidirectional switched capacitor DC-DC converter is proposed. This structure of the proposed converter allows parallel and cascade modular connection, which allows its use in different applications. The basic cell of the proposed topology is evaluated in detail in this paper. For this, characteristics of the principle of operation for step-up and step-down mode, voltage gain, voltage and current stresses, comparative evaluations with similar topologies are presented. To validate the effectiveness of the proposed converter, a prototype was built in laboratory and it achieves a 94.8 % peak efficiency with a switching frequency equal to 20 kHz.

KEYWORDS Bidirectional current flow, dc-dc converter, modular circuit, switched capacitor.

NOMENCLATURE

C_i	Capacitor, where i can be 1, 2, ... 5.
D_i	Diode, where i can be 1 or 2.
L	Inductor.
n	number of cell.
V_L	Low Voltage Bus
V_H	High Voltage Bus.
S_i	Switch, where i can be 1, 2, ... 5.
TCS	Total Current Stress.

I. INTRODUCTION

In recent years, the use of electric vehicles, renewable energy sources, such as: solar panels, fuel cells, etc, have been growing rapidly. Thus, the demand for energy storage systems to operate along with these systems has also been growing. Consequently, research involving bidirectional converters has been gaining more and more prominence.

In this context, one of the types of bidirectional converters that has been gaining popularity is the switched capacitor bidirectional converters. These converters allow the bidirectionality of the current to be done in a simple and easy way. Furthermore, in this type of converter, no magetic component (inductor or transformer) are used. So, these converters can achieve attractive volume, weight and power density. Besides that, modular connection can be applied to ensure lower current stress/ripple on components, or even increase/decrease static gain.

In power electronics, one of the first switched capacitor bidirectional converters was proposed in [1]. This converter allowed current to flow on both sides, low side (V_L) and high side (V_H). However, the voltage conversion ratio of this topology is limited to one, which means that it has low regulation capacity. In [2], a generalized modular cascading structure of bidirectional switched capacitor cells was proposed. This approach allowed to achieve a higher voltage conversion ratio. However, evaluating only one switched capacitor cell, it is evident that the voltage conversion ratio is unity. This requires a high number of cells and ends up losing the voltage regulation capacity. Using a cascaded and stacked approach, in [3], a topology of bidirectional converter to switched capacitor was proposed. This topology achieves higher voltage conversion ratio, and features compact size and weight. On the other hand, to achieve these advantages, large numbers of semiconductors are used. The Luo switched capacitor cell was used in the [4] topology. Nonetheless, it requires a considerable number of switches to achieves high voltage conversion ratio. Another combination using the Luo switched capacitor cell is proposed in [5]. This structure uses the interleaved technique to reduce the current stresses on the components. In [6] is presented the circuit design of bidirectional switched capacitor converter. The converters achieves with 2x for step-up mode and 1/2x step-down mode. Based on [3], other topologies [7]–[10] have been proposed. These approaches use the technique of stacking switched capacitor cells. A well known technique, Fibonacci Switched Capacitor was used in [11] and a bidirectional topology was proposed. This set of converters uses only capacitors and semiconductors, which they can be called pure bidirectional switched capacitor converters.

However, other combinations of bidirectional converters that use switched capacitor cells with: resonant cell [12], [13]; switched inductor [14], [15]; coupled inductor [16], etc [17], [18], have gained attention. Since they can achieve feature such as: better adjustment of voltage conversion ratio regulation; reduction of current ripple of low side (v_L) and high side (v_H) and reduction current stresses on components; soft-switching on semiconductors. In this way, these converters can improve their efficiency. However, the complexity, cost, volume of these topologies increases.

In this sense, to demonstrate that using pure switched capacitor cells can be achieved good performance, in this paper a new topology of switched capacitor bidirectional DC-DC converter is proposed. This converter has advantages such as: simplicity of operation; low number of components; low voltage stress in semiconductors; allows to increase the voltage conversion ratio from cascading cells; it allows to reduce the current stress and current ripple from parallel connection; and using the same modulation, the current flow can reverse without compromising the performance of the converter. To demonstrate these characteristics, section II presents the proposed topology and its derivations. In section III, principle of operation, static gain, voltage stress, are evaluated. Finally, experimental and simulation results, and conclusion are shown in sections IV and V, respectively.

II. PROPOSED TOPOLOGY AND ITS DERIVATIONS

In this section, the proposed topology is generated and some circuits derivations are presented. These circuits allows some advantage, such as: increase the static voltage gain for step-up ou step-down mode; the voltage and current stresses on the components decrease; and current ripple on the bus capacitors decrease.

A. Topology Generation

The three-level boost converter [19] is shown in Fig. 1(a). This converter has the advantage of increasing the voltage

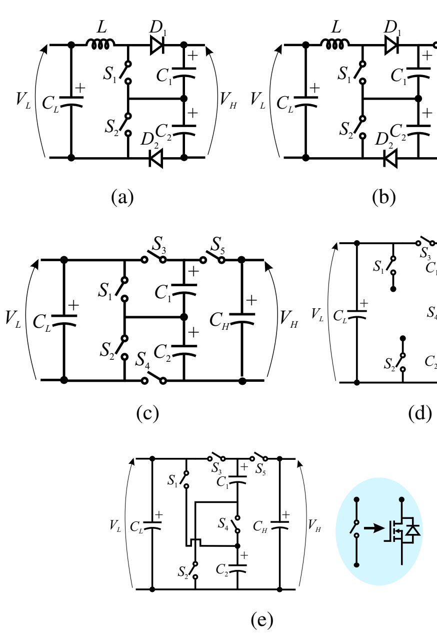


FIGURE 1. Topology derivation. (a) boost three level. (b) Step 1. (c) Step 2. (c) Step 3. (d) Step 4. (e) Proposed Converter.

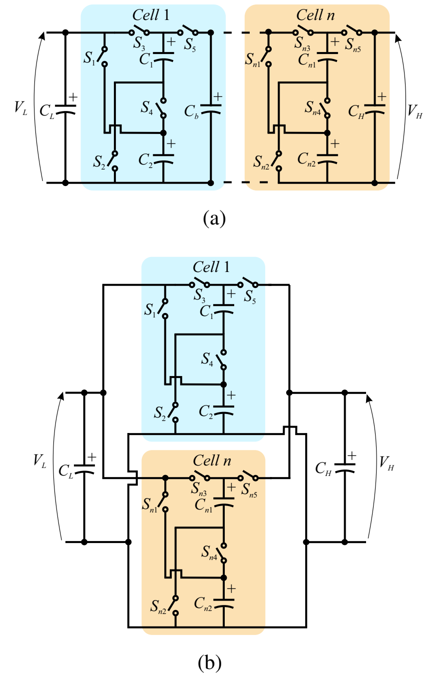


FIGURE 2. Structure of proposed converter. (a) Cascaded connection. (b) Parallel connection.

gain twice compared to traditional boost. The following steps describe how the proposed topology was generated. Initially, in the three-level boost converter was included a switch S_5 and a capacitor C_H, as can be seen in Fig. 1(b), at the output branch of the converter. To achieve a purely switched capacitor circuit, inductor L was removed from the topology. Furthermore, in this branch the diodes (D_1 and D_2) were replaced by switches (S_3 and S_4), respectively, Fig. 1(c). So to have the same reference (ground) between the voltage bus V_L and V_H , the switch S_4 was changed to the branch between the capacitors C_1 and C_2, Fig. 1(d). In sequence, to share the current I_L coming from the V_L bus and consequently reduce the current stresses on the components, the switches S_2 and S_1 were connected to the nodes "x" and "y", respectively. Thus generating the proposed topology Fig. 1(e).

The proposed converter is shown in Fig. 1(e). This converter consists of four capacitors (C_L, C_1, C_2, and C_H) and five switches (S_1, S_2, S_3, S_4 and S_5). It should be noted that the switches are MOSFETs, as can be seen on the right side of Fig. 1(e). The V_L voltage bus is the low DC voltage bus while V_H is the high DC voltage bus. This proposed cell is simple and allows different derivations to be applied to reduce stress or increase/decrease the voltage gain.

B. Topologies Derivation

The number of proposed cell can be selected according to the needs of the application. So, when the application needs high voltage conversion ratio between V_L and V_H buses, a solution is cascading the number of cells of proposed con-

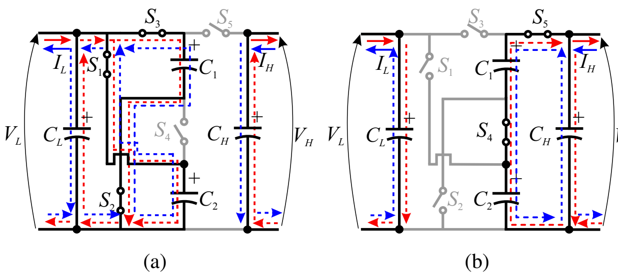


FIGURE 3. Stages of Operation. (a) First Stage (Step-up mode), Second Stage (Step-down mode). (b) Second Stage (Step-up mode), First Stage (Step-down mode).

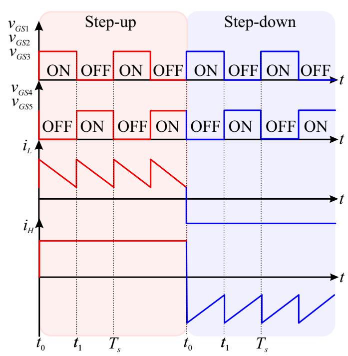


FIGURE 4. Steady state waveforms for step-up and step-down of proposed converter.

verter, as shown in Fig. 2(a), and the voltage gain increases proportionally. In other hand, to reduce the current stress and current ripple of the sources, the parallel connection, as can be seen in Fig. 2(b), can be applied. In this way, the modularity of the proposed topology is evident.

To demonstrate the theoretical and experimental evaluations, in this paper, the proposed converter (Fig. 1(e)) is analyzed.

III. PROPOSED CONVERTER EVALUATIONS

To evaluate the proposed converter, the following conditions were established: the converter operates in a steady state; the components (switches and capacitors) are considered ideal; capacitors are large enough to consider their voltages constant.

A. Principle of operation

For step-up (V_L to V_H) and step-down mode (V_H to V_L), the converter has two operation stages, Fig. 3. The main theoretical waveforms are shown in Fig. 4. As can be seen, switches S_1, S_2, and S_3 are commanded by the same PWM signal, while switches S_4, and S_5 are in the complementary PWM signal. In addition, it is possible to see the behavior of the current bus (i_L and i_H) for the step-up and step-down modes, when the bidirectional current flow occurs. To represent the current flow between V_L and V_H, two colors were used in Fig. 3.

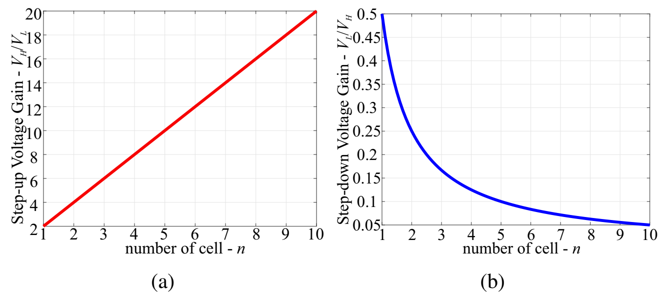


FIGURE 5. Voltage Gain. (a) Step-up mode (b) Step-down mode.

For the red color of current flow, step-up mode, the first stage is represented by Fig. 3(a), while the second stage by Fig. 3(b). In the first stage, switches S_1, S_2, and S_3 are ON while S_4, and S_5 are OFF. Capacitors C_1 and C_2 are charged up by the V_L, where $V_{C1} = V_{C2} = V_L$. Capacitor C_H is providing energy to V_H. In the second stage, switches S_4, and S_5 are ON while S_1, S_2, and S_3 are OFF. Capacitors C_1 and C_2 are discharging to V_H, where $V_H = V_{C2} + V_{C1}$.

For the blue color of current flow, step-up mode, the first stage is represented by Fig. 3(b), while the second stage by Fig. 3(a). In the first stage, switches S_4, and S_5 are ON while S_1, S_2, and S_3 are OFF. Capacitors C_1 and C_2 are charged up by the V_H, where $V_{C1} = V_{C2} = V_H/2$. Capacitor C_L is discharging to V_H. In the second stage, switches S_1, S_2, and S_3 are ON while S_4, and S_5 are OFF. Capacitors C_1 and C_2 are discharging to V_L, where $V_L = V_{C2} + V_{C1}$.

B. Voltage Gain

From the principle of operation of the proposed converter, the voltage gain can be found. For step-up mode, the voltage gain is given by:

$$\frac{V_H}{V_L} = 2n, \tag{1}$$

where n is the number of proposed cells in cascaded connection.

For step-down mode, the voltage gain is given by:

$$\frac{V_L}{V_H} = \frac{1}{2n}. \tag{2}$$

To demonstrate the behavior of voltage gains, Fig. 5 was plotted. For the step-up mode, Fig. 5(a), the voltage gain is proportional. While Fig. 5(b) for step-down mode, the voltage gain is exponential. For both cases, to increase or reduce the static voltage gain, number of switched capacitor cells must be added in cascaded.

C. Semiconductor Voltage Stress

Regarding the voltage stress on the semiconductors, they are given by:

$$V_{Si} = n_i V_L = \frac{V_{Hi}}{2n_i}, \tag{3}$$

TABLE 1. Comparative Evaluation.

Converter	Voltage Gain		Voltage Stress V_S	Current Stress	Comp. Num.	
	V_H/V_L	V_L/V_H			S	C
Proposed	2	$\frac{1}{2}$	V_L	$I_{S1(nor)} = I_{L(nor)}/2$ $I_{S2(nor)} = I_{L(nor)}/2$ $I_{S3(nor)} = I_{L(nor)}/2$ $I_{S4(nor)} = I_{H(nor)}$ $I_{S5(nor)} = I_{H(nor)}$	5	4
[1]	2	$\frac{1}{2}$	V_L	$I_{S1(nor)} = I_{L(nor)}$ $I_{S2(nor)} = I_{H(nor)}$ $I_{S3(nor)} = I_{L(nor)}$ $I_{S4(nor)} = I_{H(nor)}$	4	4
[4]	2	$\frac{1}{2}$	V_L	$I_{S1(nor)} = I_{L(nor)}$ $I_{S2(nor)} = I_{H(nor)}$ $I_{S3(nor)} = I_{L(nor)}/2$ $I_{S4(nor)} = I_{H(nor)}$ $I_{S5(nor)} = I_{L(nor)}/2$ $I_{S6(nor)} = I_{L(nor)} + I_{H(nor)}$	6	4
[6]	2	$\frac{1}{2}$	V_L	$I_{S1(nor)} = I_{L(nor)}$ $I_{S2(nor)} = I_{L(nor)}/2$ $I_{S3(nor)} = I_{H(nor)}$ $I_{S4(nor)} = I_{L(nor)}/2$ $I_{S5(nor)} = I_{H(nor)}$	5	4
[8]	2	$\frac{1}{2}$	V_L	$I_{S1(nor)} = I_{L(nor)}$ $I_{S2(nor)} = I_{H(nor)}$ $I_{S3(nor)} = I_{L(nor)}$ $I_{S4(nor)} = I_{H(nor)}$	4	3

where i can be 1, 2, 3, 4, 5, ..., $5n$.

Regarding the voltage stress on the switches, it is evident that, it is proportional as the number of cells increases.

D. Semiconductor Current Stress

The switched capacitor cell can operate in three mode: full charge, partial charge and null charge. Each one has its characteristics. However, in this paper, there is no discussion about this to demonstrate which of ones would be best to operate in the proposed converter. Therefore, the currents presented here are not standardized, as follows:

$$I_{L(nor)} = 2I_{H(nor)}, \tag{4}$$

where $I_{L(nor)}$ and $I_{H(nor)}$ are the normalized I_L and I_H current.

From this, the normalized semiconductor currents can be given by:

$$I_{S1(nor)} = I_{S2(nor)} = I_{S3(nor)} = \frac{I_{L(nor)}}{2}, \tag{5}$$

$$I_{S4(nor)} = I_{S5(nor)} = I_{H(nor)}, \tag{6}$$

Ideally, the bus powers are equal, $P_L = P_H$, and if $2V_L = V_H$, then the current I_L is higher than I_H, according to (4). As can be seen in (5), the current of these switches will always be half the current of I_L, which demonstrates low current effort. The same can be concluded for (6).

E. Comparative Evaluation

To demonstrate that the proposed converter is attractive for bidirectional converter applications, a comparative evaluation is presented in Table 1. In Table 1 only pure bidirectional switched capacitor converters are evaluated. In general, in terms of voltage gain (V_H/V_L and V_L/VH) and voltage effort on switches (V_S), all converters have the same features. Regarding the number of components, the proposed

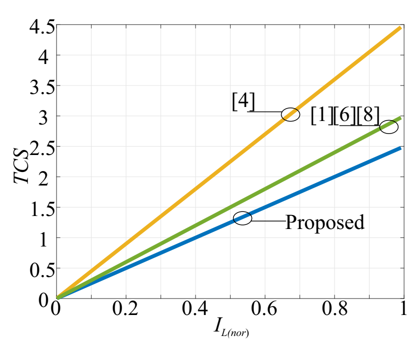


FIGURE 6. TCS Evaluation.

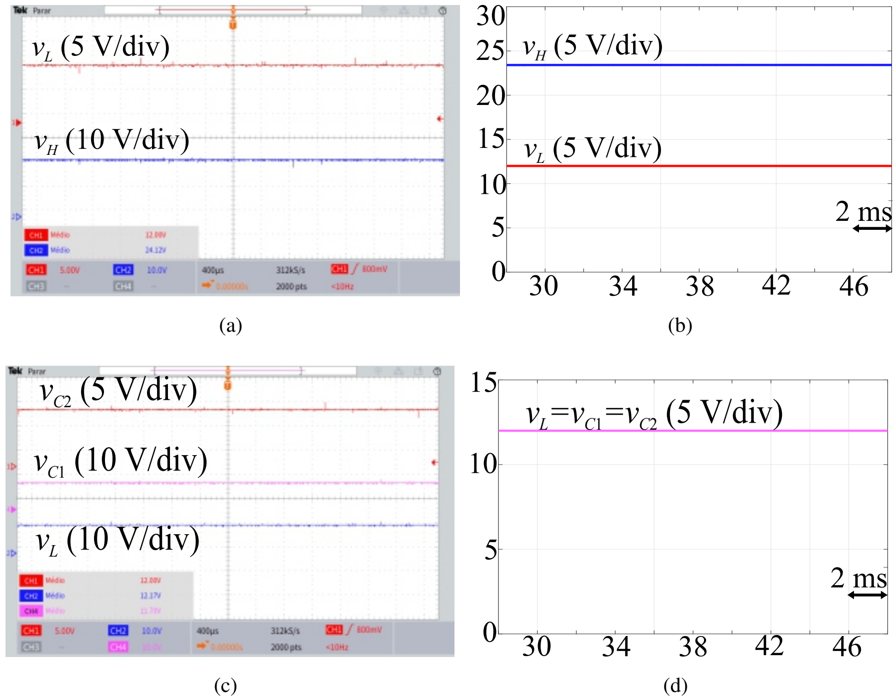


FIGURE 7. Step-up Mode waveforms of (a) v_L and v_H, Experimental. (b) v_L and v_H, Simulation. (c) v_L, v_{C1} and v_{C2}, Experimental. (d) v_L, v_{C1} and v_{C2}, Simulation.

converter is in the middle between the topologies. However, in relation to current stress, the proposed converter has better characteristics. To demonstrate this, the following approach was used.

The Total current stress factor (TCS) is basically the sum of the currents of all semiconductors and subsequently divided by the I_L current bus of the converter, as given by:

$$TCS = \frac{\sum_{i=1}^{x} I_{Si(nor)}}{I_{L(nor)}}, \tag{7}$$

where x is the maximum switch number.

For this result, the lower the TCS factor, the lower the global current stress of the converter will be and, in addition, it can be mentioned that the lower the topology conduction losses will be.

From this, Fig. 7 was plotted. As can be seen, the proposed converter presents lower TCS values for the entire $I_{L(nor)}$ range. In other words, the proposed converter has lower current stress, which implies that its conduction losses will be lower compared to the other converters since all converters have the same voltage stress on the switches ($V_S = V_L$).

1) Design Guidelines

Switched capacitor cells can operate in three modes: complete charge, partial charge and null charge. In complete charge mode, the switched capacitor cell current reaches high peak values, thus causing high switching losses. In null charge mode, the cell current is low. But the capacitors values must be high, thus, the volume and cost increase. Thus, the partial charge mode becomes attractive in terms of cost/stress [20], [21], [22]. Thus, an approach to calculate the capacities is given by:

$$C \geq \frac{0.1}{f_s(RSE + R_{DS(on)})}, \tag{8}$$

where RSE is the series equivalent resistance of the capacitor and $R_{DS(on)}$ is the Static Drain-to-Source On-Resistance. In this way, the values of the capacitors chosen for the prototype are presented in Table 2.

Regarding semiconductors, they are chosen based on the voltage and current stress presented in the previous sections. Their part numbers can be seen in the Table 2.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To demonstrate the effectiveness of the theoretical evaluations of the proposed converter, a prototype was built and tested in the laboratory. The parameters of the prototype are listed in Table 2. For these evaluations, low power was established, as the main objective is to validate operation. The proposed converter operates in open loop. It does not require any type of control to operate. To generate the PWM command signals for the switches, an STM32F103C8T6 microcontroller was used.

In order to evaluate the performance of the proposed converter, simulation and experimental results were developed. The waveforms of the obtained results are demonstrated in

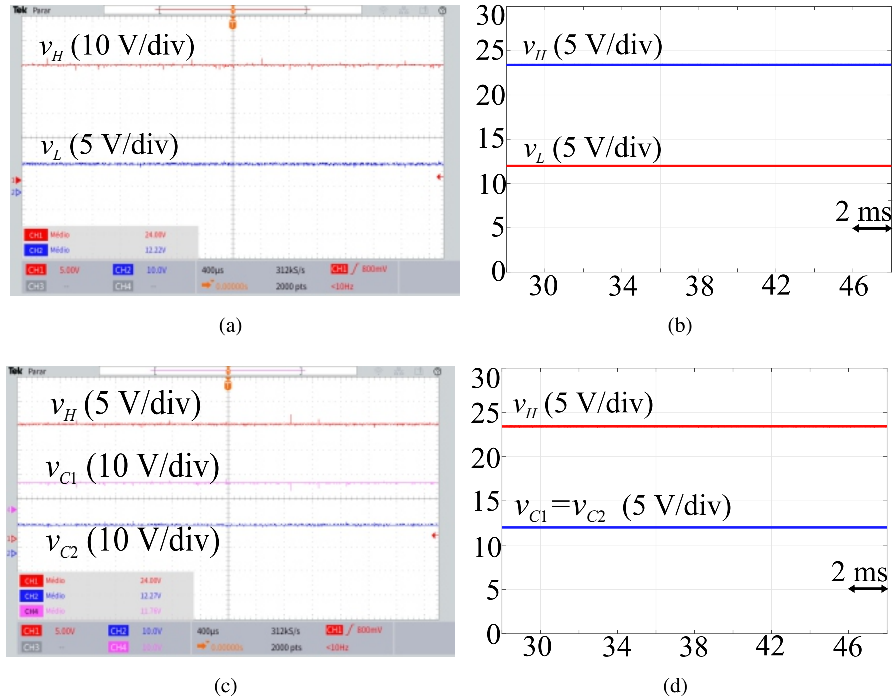


FIGURE 8. Step-down Mode waveforms of (a) v_L and v_H, Experimental. (b) v_L and v_H, Simulation . (c) v_H, v_{C1} and v_{C2}, Experimental. (d) v_H, v_{C1} and v_{C2}, Simulation .

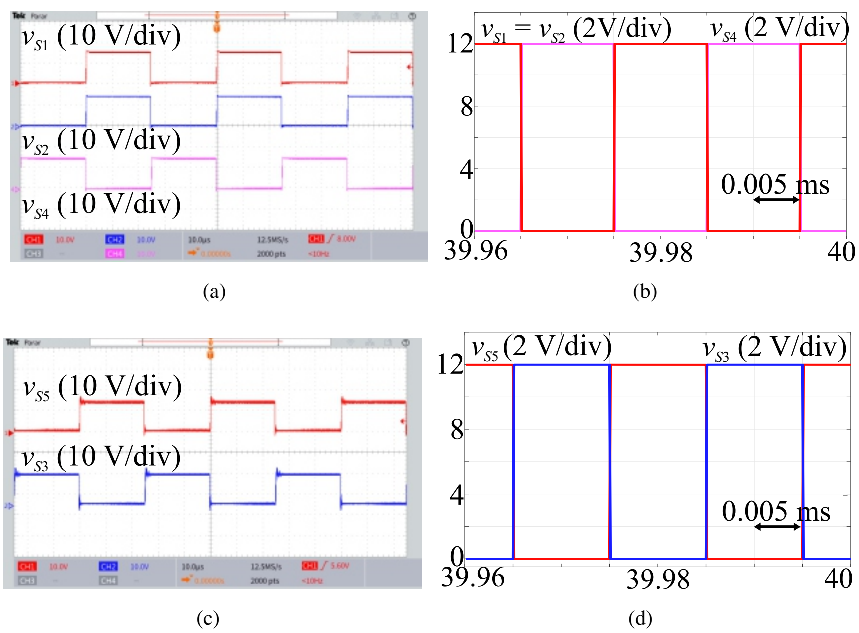


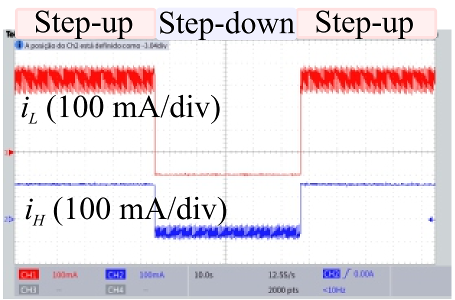
FIGURE 9. Voltage stress on semiconductors waveforms. (a) v_{s1}, v_{s2}, and v_{s4}, Experimental. (b) v_{s1}, v_{s2}, and v_{s4}, Simulation. (c) v_{s3}, and v_{s5}, Experimental. (d) v_{s3}, and v_{s5}, Simulation.

the sequence. For step-up mode, Fig. 7 shows the capacitors voltage. Fig. 7(a) and (b) show that with the input voltage (v_L = 12 V), the output voltage is v_H = 24 V, thus validating the voltage gain of the proposed converter. Furthermore, Fig. 7(c) and (d) show the voltages of capacitors C_1 and C_2, where $v_{C1} = v_{C2} = v_L$ = 12 V. In other hand, Fig. 8 shows the waveforms for step-down mode, in the same sequence. The input voltage v_H = 24 V, while $v_{C1} = v_{C2} = v_L = v_H/2$ = 12 V.

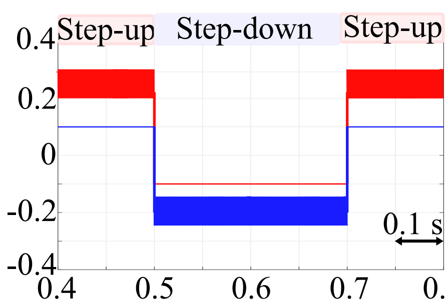
Fig. 9 presents the waveforms of voltage on semiconductors. In these results, operation stage of the proposed converter are evident and validate the theoretical waveforms.

TABLE 2. Parameters of Proposed Converter Prototype.

Symbol	Name	Value
V_H	High Voltage Bus	24 V
V_L	Low Voltage Bus	12 V
S_{all}	All Switches	IRF530N (100 V; 90 mΩ; 17 A)
C_L and C_H	Capacitors	10 μF
C_1 and C_2	Capacitors	20 μF

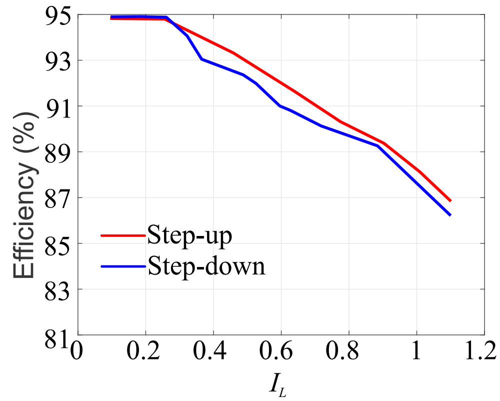


(a)

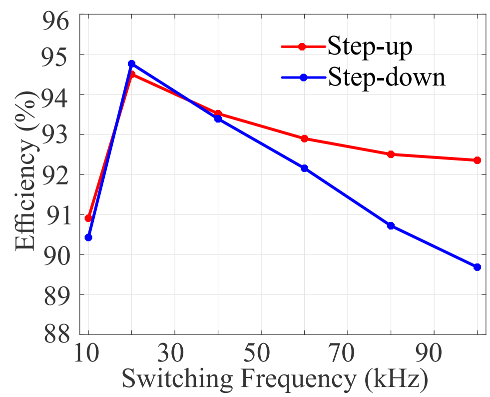


(b)

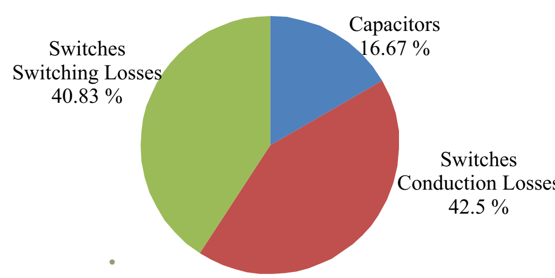
FIGURE 10. Bidirectional current flow waveforms . (a) i_L, and i_H, Experimental. (b) i_L, and i_H, Simulation.



(a)



(b)



(c)

FIGURE 11. Experimental efficiency. (a) Efficiency versus I_L. (b) Efficiency versus f_s. (c) Losses Distribution.

Also, the maximum voltage across all switches is $v_{S1} = v_{s2} = v_{S3} = v_{s4} = v_{s5} = v_L$ = 12 V, as expected.

To demonstrate the bidirectionality of current flow, Fig. 10 presents the bus currents (i_L and i_H). Initially, the converter is operating in step-up mode and is inverted to step-down mode. As can be seen, the currents i_L and i_H are positive and after the inversion of the flow, these currents become negative. Subsequently, a new inversion to step-up mode is applied. In both cases, the results presented satisfactory results.

A Yokogawa WT1800 power meter was used to extract the experimental efficiencies curves. Fig. 11 shows the efficiency of the proposed converter. The peak efficiency is approximately 94.8 % for step-down mode with a switching frequency equal to 20 kHz. As can be seen, at most points of the switching frequency, the converter achieves efficiency higher than 91 %. Overall, efficiency is always decreasing for all curves. This is due to the choice of switch used in the prototype, since the MOSFET's are for higher voltage, so the $R_{DS(on)}$ is high for Fig. 11 a). While for Fig. 11(b) it is evident that the switching losses are increasing as the switching frequency increases. To improve this, MOSFET technology must be improved. Fig. 11(c) shows the loss distribution of the proposed converter for peak efficiency. Finally, Fig. 12 shows the photograph of the prototype.

V. CONCLUSION

A pure bidirectional switched capacitor converter was proposed in this paper. The proposed converter demonstrated a good performance in terms of simplicity of operation, voltage stress, bidirectional current flow, and efficiency. Besides that, different combinations can be made with the

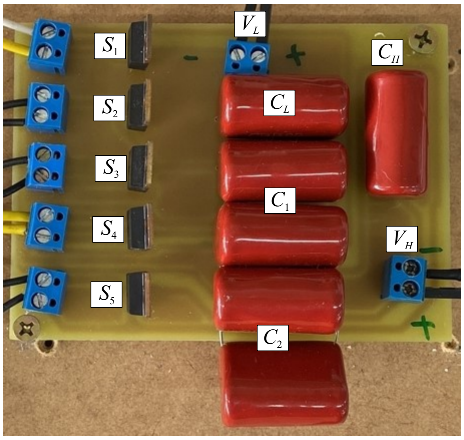


FIGURE 12. Proposed converter photograph.

proposed cell, to increase the voltage gain range, and/or decrease current stresses.

Through comparative evaluations, the proposed converter demonstrated relevance in terms of the TCS factor. This in general is an attractive advantage, since it can be said that in a certain way the conduction losses will be lower.

In terms of experimental results, the converter showed that using the same modulation strategy, the bidirectionality of the current flow presents good performance. Finally, the efficiency results are attractive but can be improved. Since lower voltage semiconductors can be used.

In general, the proposed converter can be implemented in low voltage applications that require current bidirectionality.

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AUTHOR'S CONTRIBUTIONS

NACHAU, W.A.L.: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Validation, Visualization; **VARGAS**, D.R.: Visualization, Writing – Review and Editing; **KOCH**, G.G.: Visualization, Writing – Review and Editing; **ANDRADE**, A.M.S.S.: Conceptualization, Funding Acquisition, Project Administration, Resources, Supervision, Validation, Writing – Review and Editing.

PLAGIARISM POLICY

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