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Assessment of Voltage Detection-based Selective Harmonic Current Compensation Strategies for Different Non-linear Load Signatures

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ABSTRACT This paper compares the performance of voltage detection-based selective harmonic current compensation (VDB-HCC) strategies to improve grid power quality under different non-linear load (NLL) signatures. The harmonic current compensation content of current-source and voltage-source NLLs are investigated through three VDB-HCC strategies: VDB-HCC based on a single current loop (SCL); VDB-HCC based on dual parallel current control loops (DCL); and VDB-HCC based on parallel voltage and current control loops (VCL). Analytical models and frequency response analysis are derived to corroborate the findings of this paper. Simulation results show that the VCL strategy performs better harmonic compensation compared to the SCL and DCL strategies, under penetration of both current-source and voltage-source NLLs and weak grid conditions. Experimental results using a 1.5-kW commercial distributed energy resource (DER) are also conducted. The outcomes of this paper support the decision-making of industrial consumers and distribution system operators to pursue harmonic distortion levels within acceptable limits.

KEYWORDS Harmonic current compensation, non-linear load signatures, low selective output impedance, voltage detection-based strategy, voltage distortion.

Nomenclature

ac	Alternating current
CCM	Current-controlled mode
CF	Crest factor
dc	Direct current
DCL	Dual parallel current loops
DER	Distributed energy resource
DSO	Distribution system operator
EPS	Electrical power systems
HCC	Harmonic current compensation
IIR	Infinite impulse response
MPPT	Maximum power point tracking
NLL	Non-linear load
LV	Low-voltage
PCC	Point of common coupling
PI	Proportional integral controller
PI	Proportional resonant controller
PV	Photovoltaic
PWM	Pulse-width modulation
RES	Renewable energy source
RMS	Root mean square
SCC	Short-circuit capacity
SCL	Single current loop
THD	Total harmonic distortion
TF	Transfer function
VCM	Voltage-controlled mode
VDB	Voltage detection-based
VCL	Voltage and current loops

I. INTRODUCTION

Nowadays, there is a recurring concern of the distribution system operator (DSO) regarding the high levels of harmonic content generated by non-linear loads (NLLs) into the electric power system (EPS) [1]. Although these loads individually produce low amounts of harmonic currents, their combined effect in large numbers can significantly increase voltage disturbances for both utilities and end users [2]. These power quality issues are aggravated in weak power grids and harm other grid-connected systems [3]. The widespread connection of inverter-interfaced distributed energy resources (DERs) actively allows harmonic current compensation (HCC) through available inverter-embedded power electronics [4]. HCC performed by DERs at the vicinity of NLLs mitigates the propagation of harmonic currents throughout grid nodes [5], reducing voltage distortion upstream of the compensator and benefiting both end users and utilities.

DERs can operate in current- and voltage-controlled modes (CCM and VCM, respectively) [6]. CCM DERs are widely adopted to interface intermittent renewable energy sources (RESs), such as photovoltaic (PV) and wind-based RESs. Beyond injecting active power, ancillary services can be provided by CCM DERs when using their idle power capacity. Reference [7] categorized the HCC strategies performed by CCM DERs based on the nature of the detected signal used for extracting harmonic terms: (i) current detection-based harmonic current compensation (CDB-HCC) strategies; and (ii) voltage detection-based harmonic current compensation (VDB-HCC) strategies. CDB-HCC methods rely on current measurements, requiring downstream grid current or load current measurements (i.e., an extra current sensor), and are not straightforward under multiple dispersed loads, as in microgrids. On the other hand, VDB-HCC strategies extract harmonic components from the DER point of common coupling (PCC) voltage, using only embedded measurements and control loops to reshape DER output impedance at selective harmonic frequencies.

References [8]–[11] address CDB-HCC strategies applied to CCM DERs, while references [12]–[16] show the VDB-HCC strategies applied to CCM DERs. In the authors' previous work [7], a comprehensive comparison of three VDB-HCC strategies was assessed: VDB-HCC based on a single current loop (SCL) [12], [13]; VDB-HCC based on dual parallel current control loops (DCL) [14]; and VDB-HCC based on parallel voltage and current control loops (VCL) [15], [16]. The VDB-HCC strategies were compared in terms of MPPT static efficiency, voltage distortion improvement under stiff and weak grids, computational burden, transient settlement time, and transient current overshoot. VCL has shown the best performance in terms of voltage distortion reduction under weak grids. Despite the several figures of merit computed in [7], there is a lack of technical literature discussing and comparing VDB-HCC strategies mitigating harmonic currents drained by different NLL signatures. NLLs are classified herein as current-source or voltage-source NLL [17], [18]. For motor-based loads, the inductances of the motors restrict the rate of current change. This feature of the current-source NLL confers the behavior of harmonic current source to these loads. For rectifiers with dc output capacitors, voltage changing rate limitation is imposed by the dc capacitor, conferring the behavior of a harmonic voltage source to this NLL.

Thus, this paper evaluates the performance of the SCL, DCL, and VCL strategies for both types of NLLs: voltage-source and current-source NLLs. The sharing of harmonic currents between the grid and DERs embedded with VDB-HCC strategies is addressed by means of the frequency response metric and time-varying results. Also, experimental results considering NLL voltage- and current-source NLLs are conducted in an experimental setup composed of a 1.5-kW commercial DER. Since current-source and voltage-source NLLs are mostly found in industries and homes, respectively, this paper supports the decision-making of industrial consumers and DSOs to pursue harmonic distortion levels within acceptable limits through the most appropriate VDB-HCC strategy.

This paper is outlined as follows: Section II presents the description and the background of the voltage detection-based HCC strategies. Section III shows the rectifier-based non-linear load signatures and addresses the performance of VDB-HCC strategies under such penetration of different NLL types. Section IV and Section V show comparative simulation and experimental results, respectively. Conclusions are stated in Section V.

II. VOLTAGE DETECTION-BASED HCC STRATEGIES

Figure 1(a) shows a schematic of a typical single-phase grid-connected H-bridge DER, with LC filter. The upstream grid (220 V and 60 Hz) is modeled with low short-circuit capacity (SCC = 40 kVA), through the line impedance Z_g (R_g = 0.9 Ω and L_g = 2 mH) and grid voltage v_g. A low-voltage (LV) with this SCC comprises a weak grid. An NLL is connected at the DER PCC. The inverter control diagram is shown in Figure 1(b), composed of cascaded loops: slower outer loops (Q and v_{dc}); and faster inner current loop, where the VDB-HCC strategies are implemented. The switch at positions ⓪,

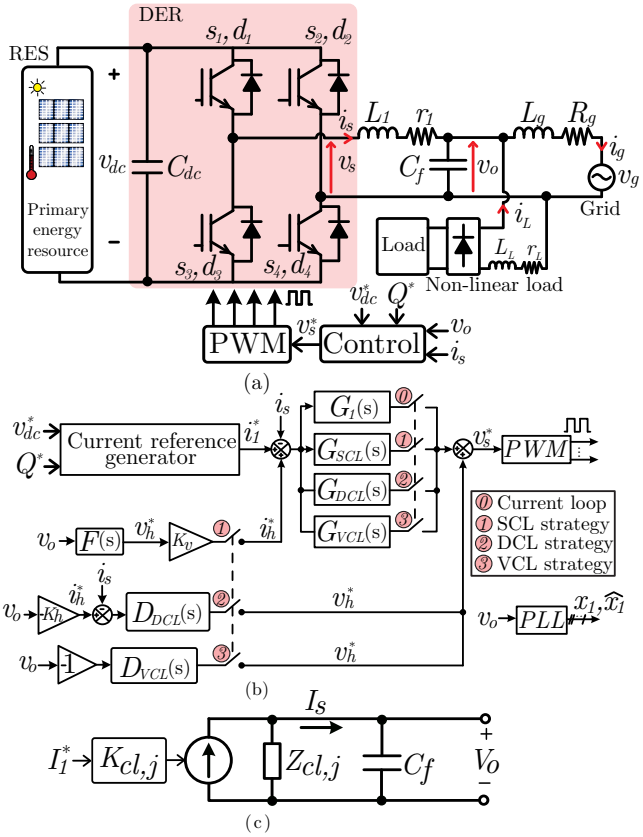

FIGURE 1. (a) Single-phase grid-connected DER. (b) Inverter control diagram for current control, SCL, DCL, and VCL strategies. (c) Norton circuit-equivalent model of the DER.

TABLE 1. Transfer functions related to (1) and Fig. 1(c).

TF	Equation	Parameter
$K_{cl,CL}$(s)	$\frac{G_1 \cdot H}{Z_1+G_1 \cdot H}$	Z_1(s): DER filter impedance H(s): PWM and the digital delay G_1(s): Current fund. PR controller
$Y_{cl,CL}$(s)	$\frac{1}{Z_1+G_1 \cdot H}$	
$K_{cl,SCL}$(s)	$\frac{G_{SCL} \cdot H}{Z_1+G_{SCL} \cdot H}$	G_{SCL}(s): multi-PR SCL controller F(s): IIR selective filters K_v: SCL adjustable gain (1/Ω)
$Y_{cl,SCL}$(s)	$\frac{1+G_{SCL} \cdot H \cdot F \cdot K_v}{Z_1+G_{SCL} \cdot H}$	
$K_{cl,DCL}$(s)	$\frac{G_{DCL} H}{Z_1+(G_{DCL}+D_{DCL})H}$	$G_{DCL}(s)$: fund. PR DCL controller D_{DCL}(s): multi-PR DCL controller K_h: DCL adjustable gain (1/Ω)
$Y_{cl,DCL}$(s)	$\frac{1+D_{DCL} \cdot H \cdot K_h}{Z_1+(G_{DCL}+D_{DCL})H}$	
$K_{cl,VCL}$(s)	$\frac{G_{VCL} \cdot H}{Z_1+G_{VCL} \cdot H}$	G_{VCL}(s): fund. PR VCL controller D_{VCL}(s): multi-PR VCL controller
$Y_{cl,VCL}$(s)	$\frac{1+D_{VCL} \cdot H}{Z_1+G_{VCL} \cdot H}$	

①, ②, and ③ selects the following inner loop strategies: without VDB-HCC (i.e., current control or CL), SCL, DCL, and VCL methods, respectively.

The SCL strategy is formed by a single current loop, in which fundamental current tracking and HCC are performed simultaneously by the same controller (i.e., G_{SCL}). The DCL strategy comprises dual parallel current loops, in which controllers G_{DCL} and D_{DCL} are employed in each loop. Similarly, the VCL strategy comprises two parallel loops, where controllers G_{VCL} and D_{VCL} are employed. However, the HCC loop is based on voltage signals, whereas the fundamental reference tracking loop is based on current amounts. The VDB-HCC strategies are fairly compared herein, with the core idea of the methods preserved without loss of generality. Following the guidelines and assumptions described in [7], the system closed-loop response generalized for any VDB-HCC strategy is given by:

$$I_s(\mathrm{s}) = I_1^*(\mathrm{s}) \cdot K_{cl,j}(\mathrm{s}) - V_o(\mathrm{s}) \cdot Y_{cl,j}(\mathrm{s}), \tag{1}$$

where $K_{cl,j}$ represents the closed-loop response of DER current (I_s) to fundamental reference (I_1^*) for the j-th VDB-HCC strategy. $Y_{cl,j} = 1/Z_{cl,j}$ indicates the DER output admittance I_s/V_o for j-th VDB-HCC strategy. Subscript $j = \{\mathrm{CL}, \mathrm{SCL}, \mathrm{DCL}, \mathrm{VCL}\}$ indicates which strategy is adopted. The closed-loop model of (1) is represented by an equivalent Norton circuit shown in Figure 1(c). Table 1 summarizes the transfer functions (TFs) $K_{cl,CL}$, $K_{cl,SCL}$, $K_{cl,DCL}$ and $K_{cl,VCL}$ for each VDB-HCC strategy, as well as the DER output admittance (i.e., $Y_{cl,CL}$, $Y_{cl,SCL}$, $Y_{cl,DCL}$ and $Y_{cl,VCL}$). Also, $Z_1 = r_1 + sL_1$ is the impedance of the converter-side inductor. H(s) is a first-order TF representing the pulse width modulation (PWM) and the digital implementation delay [8]. F(s) models selective infinite impulse response (IIR) filters applied in SCL strategy for extracting the harmonic components of V_o [7]. As shown analytically in Table 1, VDB-HCC strategies affect the DER output impedance by creating virtual selective low-impedance paths for harmonics [7]. The controllers of each strategy are defined in (2)-(5):

$$G_1(s) = k_p + \frac{k_{r,1} s}{s^2 + (\omega_n)^2}, \tag{2}$$

$$G_{SCL}(s) = k_p + \sum_h \frac{k_{r,h} s}{s^2 + (h\omega_n)^2}, \tag{3}$$

$$G_{DCL}(s) = k_p + \frac{k_{r,1} s}{s^2 + \omega_n^2},\ D_{DCL}(s) = \sum_h \frac{k_{r,h} s}{s^2 + (h\omega_n)^2}. \tag{4}$$

$$G_{VCL}(s) = k_p + k_{r,1} \frac{s}{s^2 + \omega_n^2},\ D_{VCL}(s) = \sum_h \frac{k_{r,h} s}{s^2 + (h\omega_n)^2}. \tag{5}$$

where ω_n is the fundamental angular frequency. h is the set of tuned harmonic orders, when applicable. k_p and $k_{r,h}$ are the proportional and resonant gains of current controllers, respectively, equally tuned when applicable. The SCL and DCL strategies rely on scaling the K_v and K_h gains, both tuned according to the guidelines of [7] (i.e., 1.09 and 4.63 Ω^{-1}, respectively) for wide grid impedance variation.

III. PERFORMANCE OF VDB-HCC STRATEGIES FOR DIFFERENT NLL SIGNATURES

A. Rectifier-based non-linear loads

Figure 2 shows the non-controlled rectifier-based load signatures, considering three types of loads: (a) resistive, (b) capacitive or voltage-source, and (c) inductive or current-source. Figure 2(d) shows the voltage v_o and current i_L waveforms drained from the grid by the three load types, while Figure 2(e) shows the harmonic spectrum content of the currents shown in Figure 2(d). Subscripts $_1$, $_2$, and $_3$ are used for parameters related to resistive, capacitive, and inductive loads, respectively.

For the resistive load of Figure 2(a), the input voltage and current waveforms have the same phase and sinusoidal shape. Figure 2(e) shows only 1.77 A of the fundamental current component. For the voltage-source NLL of Figure 2(b), the waveform of the input current $i_{L,2}$ is very distorted, presenting pulses with very high $\frac{di_{L,2}}{dt}$ during capacitor $C_{L,2}$ recharging. The harmonic spectrum of Figure 2(e) shows high current magnitudes at odd line-frequency multiple harmonic components. Finally, the load in Figure 2(c) behaves as a current source, draining an almost squared input current $i_{L,3}$. Figure 2(e) shows that the input NLL current spectrum of Figure 2(c) also contains odd line-frequency multiple harmonic components, with considerably smaller magnitudes compared to voltage-source NLL. Load parameters are sized to absorb approximately the same fundamental current signature, where the chosen RLC components are based on laboratory availability for experimental evaluation. The crest factor (CF) for the RC load is $CF_2 = \frac{I_{L,2}^{pk}}{I_{L,2}^{rms}} = \frac{6.27}{2.39} \approx 2.62$,

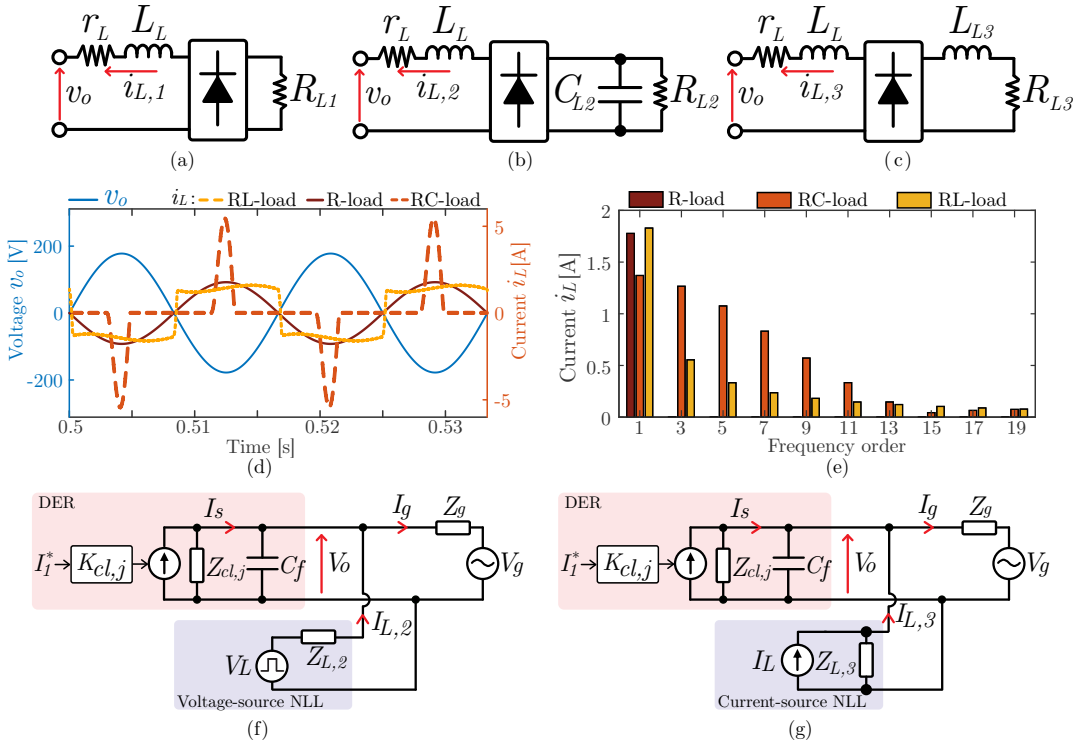

FIGURE 2. Rectifier-based load signatures, considering (a) resistive load, (b) capacitive or voltage-source load, and (c) inductive or current-source load. (d) Input voltage and current waveforms. (e) ac current harmonic spectrum. R_{L2}=250 Ω, R_{L1}=125 Ω, and R_{L3}=100 Ω for the voltage-source, resistive, and current-source loads. C_{L2}=0.2 mF and L_{L3}=500 mH. (f) Equivalent circuit of the DER, voltage-source NLL, and upstream grid. (g) Equivalent circuit of the DER, current-source NLL, and upstream grid.

$$\text{Voltage-source NLL}: \; I_g = \frac{K_{cl,j}}{Z_g(Z_{cl,j}^{-1}+Z_{L,2}^{-1}+Z_g^{-1})}I_1^* + \frac{1}{Z_g Z_L(Z_{cl,j}^{-1}+Z_{L,2}^{-1}+Z_g^{-1})}V_L + \frac{1-Z_g(Z_{cl,j}^{-1}+Z_{L,2}^{-1}+Z_g^{-1})}{Z_g^2(Z_{cl,j}^{-1}+Z_{L,2}^{-1}+Z_g^{-1})}V_g. \tag{6}$$

$$\text{Current-source NLL} \; : \; I_g = \frac{K_{cl,j}}{Z_g(Z_{cl,j}^{-1}+Z_g^{-1})}I_1^* + \frac{1}{Z_g(Z_{cl,j}^{-1}+Z_g^{-1})}I_{L,3} + \frac{1-Z_g(Z_{cl,j}^{-1}+Z_g^{-1})}{Z_g^2(Z_{cl,j}^{-1}+Z_g^{-1})}V_g. \tag{7}$$

which comprises an NLL with high harmonic content. The CF for the RL load is $CF_3 = \frac{I_{L,3}^{pk}}{I_{L,3}^{rms}} = \frac{2.28}{1.95} \approx 1.17$, as this low value is inherent to this type of NLL.

B. Harmonic compensation capability for different NLL signatures

Reference [19] addressed the voltage-source NLL by an equivalent Thévenin circuit, in which the distorted voltage source is modeled by V_L and the series impedance by $Z_{L,2}$ - vide Figure 2(f). Also, the current-source NLL is approximated by a Norton equivalent circuit [19], in which the distorted current source is modeled by I_L and the parallel impedance by $Z_{L,3}$ - vide Figure 2(g). Figure 2(f) shows the equivalent circuit of the DER, voltage-source NLL, and upstream grid, while Figure 2(g) shows the same equivalent circuit for the current-source NLL. Due to the high impedance for low frequencies (< 1 kHz), the LC filter capacitor C_f is neglected without loss of generality [20]. From Figures 2(f) and (g), the grid current I_g is written as a function of V_L, V_g, $I_{L,3}$ and I_1^*, as derived in (6) and (7) for voltage-source and current-source NLL, respectively. The contributions of DER and voltage-source NLL to the grid current essentially depend on the Z_g, $Z_{L,2}$ and $Z_{cl,j}$. On the other hand, the contributions of the DER and current-source NLL to compose I_g depend on Z_g and $Z_{cl,j}$.

Assuming an upstream grid with high SCC (i.e., SCC $\rightarrow \infty$, or $Z_g \rightarrow 0$), (6) and (7) are given by:

$$I_g\Big|_{Z_g=0} = K_{cl,j}\cdot I_1^* + \frac{V_L}{Z_{L,2}}, \tag{8}$$

$$I_g\Big|_{Z_g=0} = K_{cl,j}\cdot I_1^* + I_{L,3}, \tag{9}$$

where $K_{cl,j}$ behaves as a low-pass filter up to the DER current control bandwidth, regardless of the j-th VDB-HCC

TABLE 2. Parameters of the DER, NLLs, and upstream grid (see Fig. 1).

DER parameters	Label	Value
Inverter rated active power	P_n	1.5 kW
Switching/sampling frequency	f_{sw}, f_s	20 kHz
LC filter impedance	L_1, r_1	2 mH, 77.10 mΩ
LC filter capacitance	C_f	3.3 μF
Grid voltage (RMS)	V_g	220 V
Grid impedance	L_g, R_g	2 mH, 0.9 Ω
Grid short-circuit capacity	SCC	40 kVA
Grid angular frequency	ω_n	377 rad/s
dc-link voltage reference	v_{dc}^*	400 V
dc-link capacitance	C_{dc}	1.17 mF
NLL parameters	**Label**	**Value**
Voltage-source NLL	R_{L2}, C_{L2}	250 Ω, 0.2 mF
Current-source NLL	R_{L3}, L_{L3}	100 Ω, 500 mH
Resistive NLL	R_{L1}	125 Ω
NLL connection impedance	L_L, r_L	2 mH, 1 Ω
DER controller parameters	**Label**	**Value**
HCC selective harmonic orders	h	3, 5, 7, 9, 11
Inner loop: cutoff frequency	f_c	1.2 kHz
Inner loop: phase margin	PM	90°
Inner loop: Proportional gain	k_p	25 Ω
Inner loop: Resonant gain	$k_{r,1}$	1000 Ω/s
Inner loop: Harm. resonant gain	$k_{r,h}$	500 Ω/s
IIR filter bandwidth	f_b	2 Hz
SCL adjustable gain	K_v	1.09 Ω^{-1}
DCL adjustable gain	K_h	4.63 Ω^{-1}

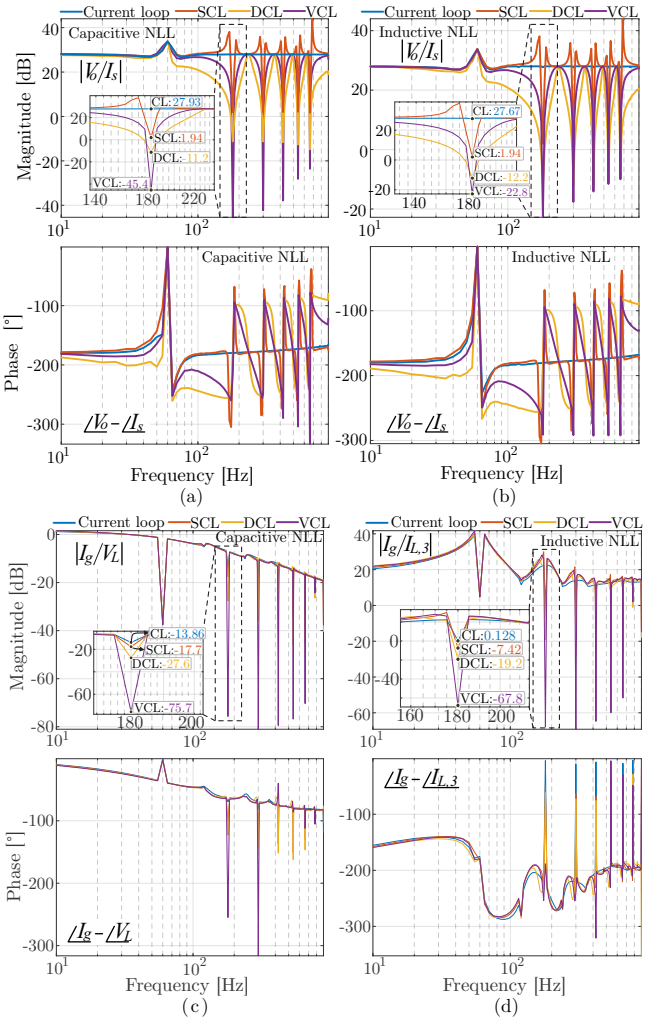

FIGURE 3. Frequency response of the DER output impedance, considering the penetration of: (a) voltage-source NLL; (b) current-source NLL. Frequency response of HCC effectiveness metrics by VDB-HCC strategies for (c) voltage-source NLL (i.e., I_g/V_L) and (d) current-source NLL (i.e., $I_g/I_{L,3}$).

strategy [7]. In both cases, I_g is composed of the NLL current (i.e., $I_{L,3}$ or $V_L/Z_{L,2}$) and the DER fundamental current I_1^*. Thus, the DER equipped with the VDB-HCC strategies is not able to perform HCC if $Z_g \to 0$, regardless of the NLL type. This very important result suggests that VDB-HCC are suitable for weak grids, which is typically the case of LV distribution grids. For stiff grids, CDB-HCC strategies provide an alternative solution for HCC, despite the requirement regarding the new current sensor to measure the NLL current.

In view of the aforementioned, the closed-loop system of Figure 1(a) is simulated for each VDB-HCC strategy embedded in the DER, considering the penetration of current-source and voltage-source NLLs. Table 2 shows the main parameters of the DER, NLLs, and upstream grid. It should be reinforced that the simulation involved switched DER with its appropriate control loops and electronic circuit of the NLLs. An ac frequency sweep analysis from 10 Hz - 900 Hz is performed with a resolution of 5 Hz, and the obtained frequency responses are shown in Figure 3. For instance, Figures 3(a) and (b) show the frequency response of the DER output impedance (i.e., V_o/I_s) for the strategies without VDB-HCC (i.e., current loop), SCL, DCL, and VCL, considering (a) voltage-source and (b) current-source NLLs. A high DER output impedance at the fundamental frequency is noted for all strategies. On the other hand, selective virtual low-impedance paths (i.e., h={3, 5, 7, 9, 11}) for harmonics are created when SCL, DCL and VCL strategies are implemented. The behavior of the DER output impedance in Figures 3(a) and (b) is similar regardless of the grid-connected NLL type. Furthermore, the DER impedance notches at the selective frequencies are deeper according to the following order of strategies: VCL, DCL, and SCL. Thus, VCL is expected to be more effective HCC for both NLL loads.

According to [19], the effectiveness of HCC can be computed by the ratio I_g/V_L and $I_g/I_{L,3}$ for voltage-source and current-source NLLs, respectively. Improved HCC performance is achieved when there is a lower level of distorted current circulation from the NLL to the grid, which corresponds to lower values of I_g/V_L or $I_g/I_{L,3}$ at the HCC selective frequencies. Figures 3(c) and (d) show

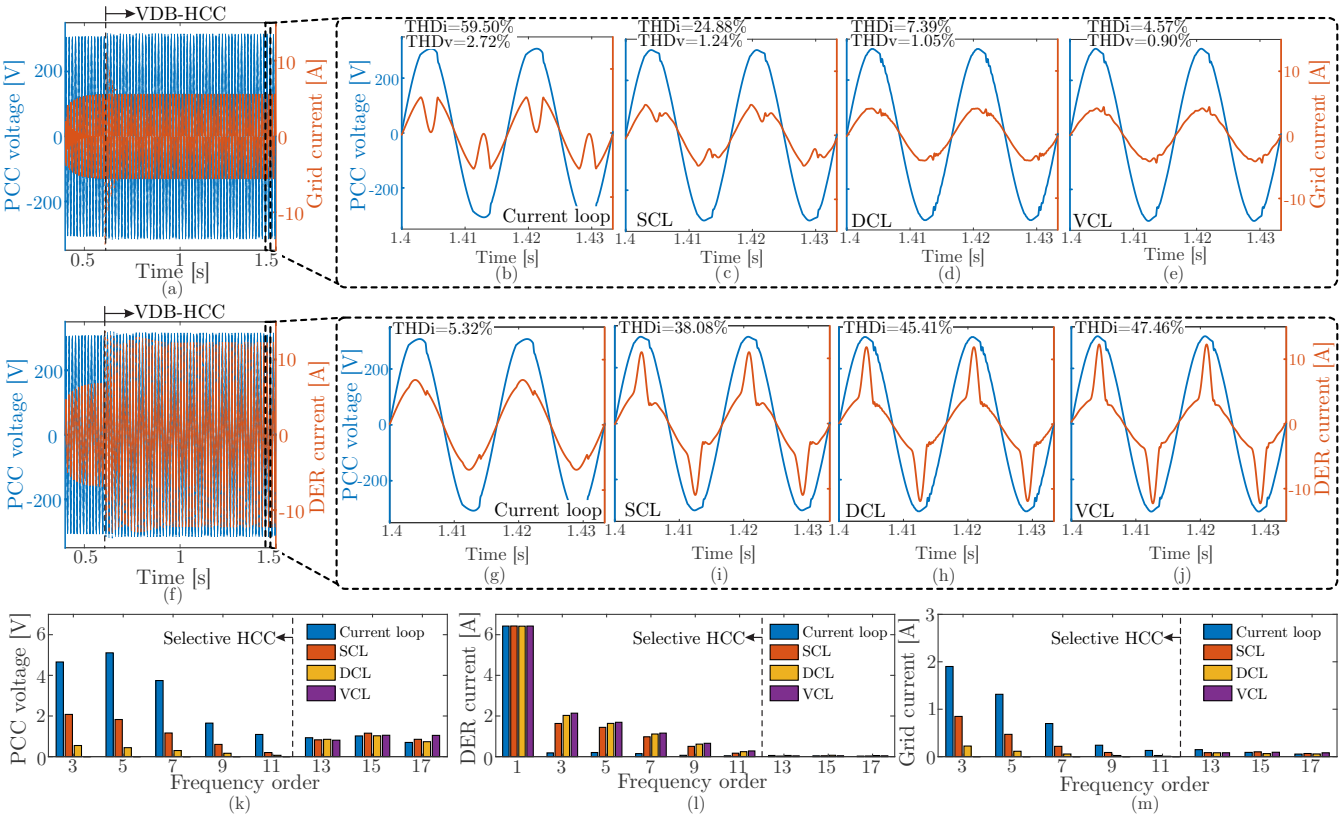

FIGURE 4. Voltage-source NLL: (a) PCC voltage and grid current, where the zoomed views show the following scenarios: (b) without VDB-HCC; (c) SCL; (d) DCL; and (e) VCL strategies. (f) PCC voltage and DER current, where the zoomed views highlight the scenarios: (g) without VDB-HCC; (h) SCL; (i) DCL; and (j) VCL strategies. (k) PCC voltage, (l) DER current, and (m) grid current harmonic spectra at t = 1.4 s.

the frequency response of (c) I_g/V_L for voltage-source NLL and (d) $I_g/I_{L,3}$ for current-source NLL, considering the strategies without VDB-HCC (i.e., current loop), SCL, DCL, and VCL strategies. For both NLLs, the DER embedded with VDB-HCC strategies inserts h-th selective notches to I_g/V_L and $I_g/I_{L,3}$, which is not observed for the case without VDB-HCC. Through the comparison between the VDB-HCC strategies, the same conclusions obtained in Figures 3(a) and (b) are valid for Figures 3(c) and (d), where the VCL strategy presents better HCC performance due to deeper frequency notches. Comparing the VDB-HCC strategies among the two types of NLL, VDB-HCC methods are more effective for voltage-source NLL under the adopted grid impedance condition. This conclusion is obtained by comparing the results of Figures 3(c) and (d), in which the I_g/V_L ratio at selective HCC frequencies has a smaller magnitude compared to $I_g/I_{L,3}$. At 180 Hz (i.e., $h = 3$), a reduction from 0.13 dB to -13.86 dB, from -7.43 dB to -17.70 dB, from -19.2 dB to -27.60 dB, and from -67.80 dB to -75.70 dB are observed comparing Figures 3(c) and (d) for the current loop, SCL, DCL and VCL strategies, respectively. This behavior is analogous to the other HCC selective frequencies. Although voltage-source NLL exhibits a more pronounced harmonic spectrum compared to current-source NLL - see Figure 2(e), HCC performed by VDB-HCC strategies are more effective for this voltage-source NLL in such simulation conditions.

IV. SIMULATION RESULTS

The same parameters for the DER, NLLs, and upstream grid listed in Table 2 are adopted. PLECS® platform is adopted in the simulations, with a discrete simulation step of 0.83 μs. All VDB-HCC strategies are fairly compared during steady-state time-varying response, considering the controller parameters addressed in Table 2. Current and voltage meters are simulated according to polarities shown in Figure 1. For the SCL strategy, selective IIR filters with a bandwidth of 2 Hz are adopted.

A. Voltage-source NLL

The current and voltage waveforms considering the grid voltage distorted by the voltage-source NLL are shown in Figures 4(a)-(j), where THD values are also reported. Four scenarios are conducted in the simulation results of Figure 4 regarding the strategies shown in Figure1(b): (i) Case without VDB-HCC, with the current control formed only by PR tuned to the fundamental frequency; (ii) Case with SCL strategy (iii) Case with DCL strategy; (iv) Case

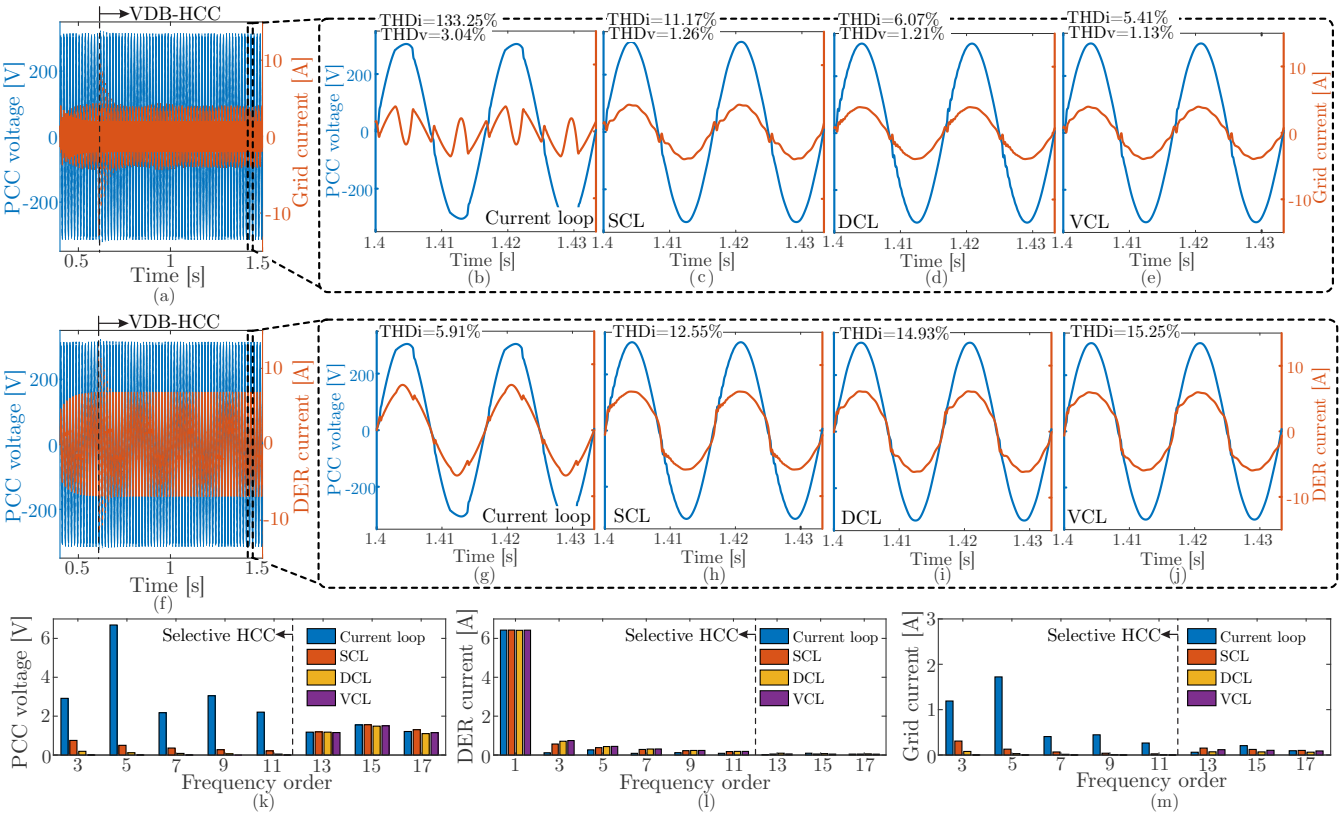

FIGURE 5. Current-source NLL: (a) PCC voltage and grid current, where the zoomed views show the scenarios: (b) without VDB-HCC; (c) SCL; (d) DCL; and (e) VCL strategies. (f) PCC voltage and DER current, where the zoomed views highlight the scenarios: (g) without VDB-HCC; (h) SCL; (i) DCL; and (j) VCL strategies. (k) PCC voltage, (l) DER current, and (m) grid current harmonic spectra at t=1.4 s.

with VCL strategy. VDB-HCC strategies are all enabled at 0.6 s. The transient initialization of VDB-HCC strategies is investigated in [7], in which SCL presented the best transient response followed by DCL and VCL.

Figures 4(b)-(e) show the zoomed view of the PCC voltage (v_o) and grid current (i_g) acquired at 1.4 s for the scenarios without VDB-HCC, with SCL, DCL, and VCL strategies, respectively. Figures 4(g)-(j) show the zoomed view of the PCC voltage (v_o) and DER current (i_s) for the scenarios without VDB-HCC, with SCL, DCL, and VCL strategies, respectively. When the VDB-HCC strategies are enabled, the 3rd, 5th, 7th, 9th, and 11th selective harmonics are attenuated, resulting in the PCC voltage THD reduction. The VCL, DCL, and SCL strategies reduced the PCC THD voltage from 2.72% to 1.24%, 1.05%, and 0.90%, respectively. Since the harmonic components introduced by the NLL flow through the inverter arms rather than to the grid, the DER current THD increases from 5.32% to 45.41%, 38.08%, and 47.46% for VCL, DCL, and SCL strategies, respectively - see Figure 4(l). On the other hand, the grid current THD significantly reduces from 59.50% to 7.39%, 24.88%, and 4.57% when enabling the SCL, DCL, and VCL strategies, respectively - see Figure 4(m). Due to selective compensation up to the 11th harmonic order, no reduction of h>11 components are noticed in Figures 4(k)-(m). Especially for the VCL strategy, the PCC voltage harmonic distortion significantly reduces due to the low-impedance path created by this VDB-HCC strategy.

B. Current-source NLL

Figures 5(a)-(j) show the current and voltage waveforms considering the grid voltage distorted by the current-source NLL. The same previous simulation events are performed herein, except for changing the voltage-source to current-source NLL. The zoomed view of Figures 5(b)-(e) shows that the PCC voltage THD reduces from 3.04% to 1.26%, 1.21%, and 1.13%, when enabling SCL, DCL, and VCL methods, respectively. On the other hand, the DER current THD increases from 5.91% to 12.55%, 14.93%, and 15.25%; and the grid current THD significantly reduces from 133.25% to 11.17%, 6.07%, and 5.41% when enabling the SCL, DCL, and VCL strategies. Figures 5(k)-(m) show the harmonic spectra of PCC voltage, DER current, and grid current, respectively. As noted, a significant reduction in the selective harmonic content (i.e., h=$\{3, 5, 7, 9, 11\}$) of PCC voltage and grid current of harmonic order is observed.

Finally, comparing the results of Figures 4 and 5, HCC performed by VDB-HCC strategies is more effective for

FIGURE 6. Laboratory-scaled experimental prototype. The diagram connection of each piece of equipment is established in Figure 1.

the voltage-source NLL, even with the voltage-source NLL exhibiting a more pronounced harmonic spectrum in comparison to the current-source NLL. This result is in agreement with the discussions performed in Section III.

V. EXPERIMENTAL RESULTS

Experiments have been developed on a 1.5-kW PHB 1500-NS commercial DER hardware, in which programming is performed on the TMS320F28034 fixed-point digital signal processor. The system parameters are the same as shown in Table 2, including DER and both NLL types. The laboratory-scaled experimental prototype is shown in Figure 6. Further details of the experimental setup can be found on [21]. The 20 kW TC.GSS DC power source supplies the voltage to the dc-side of the DER. The TC-ACS 30 kVA programmable four-quadrant grid emulator is connected to the ac-side of the inverter. Signal measurements are obtained from a 4-channel oscilloscope equipped with A612 and P5200A probes.

As shown in Section IV, the VCL strategy shows superior steady-state performance in selective HCC compensation and voltage THD improvement for both NLL types. Thus, the following results compare the VCL strategy with the case without VDB-HCC (i.e., current control). The experimental time-varying waveforms for both control strategies and NLL types are shown in Figures 7, where THD values, PCC voltage (v_o) and grid (i_g), DER (i_s) and NLL (i_L) currents are reported. The injected DER current without VDB-HCC strategy shows a considerable THDi because the PCC voltage is distorted and the DER processes just 20% of its fundamental rated current. The DER current control disturbance occurs especially at moments of high di/dt of NLL loads. Figures 7(a)-(b) show the steady-state selective HCC performance of VCL compared to current control for voltage-source NLL penetration into the grid. The PCC voltage THD reduces from 2.39% to 1.12%, when enabling the VCL method. The DER current THD increases from 15.4% to 44.28%, and the grid current THD reduces from 32.34% to 10.04% when enabling the VCL strategy.

Figures 7(c)-(d) show the time-varying waveforms for the current control and VCL strategies, considering the current-

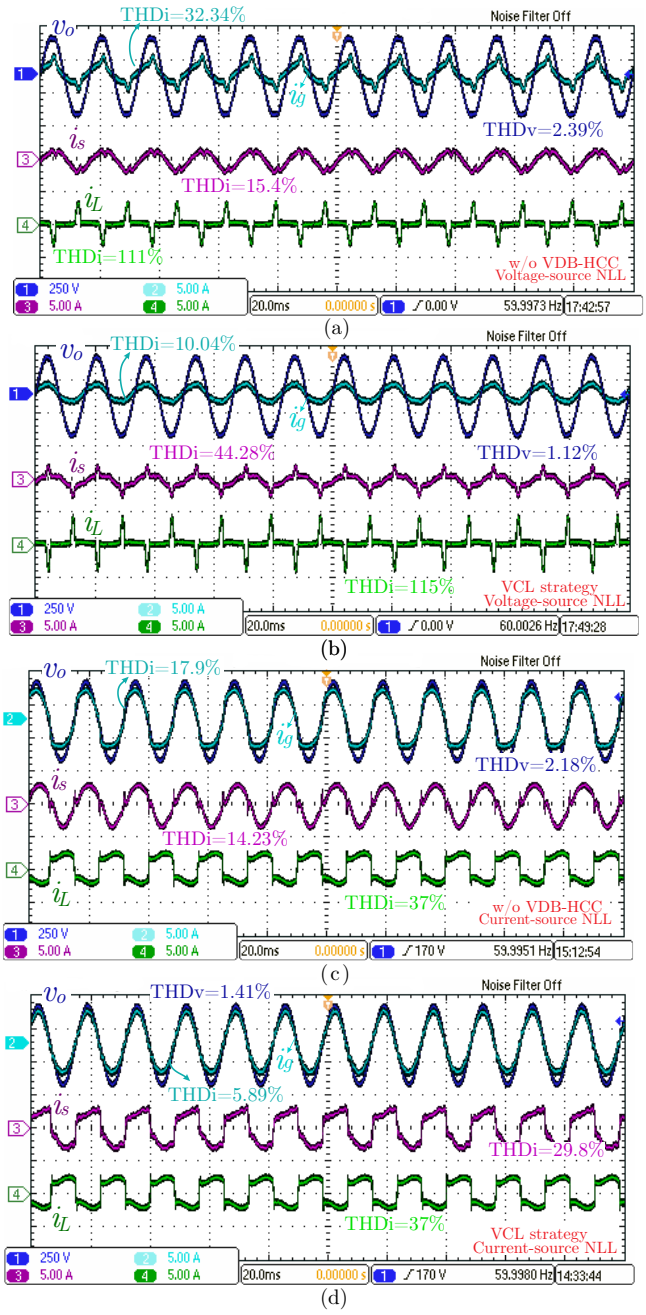

FIGURE 7. Experimental results for the commercial DER connected to a grid with SCC of approximately 40 kVA (PCC voltage [250 V/div], grid current [5 A/div], DER current [5 A/div]; NLL current [5 A/div]; and time [20 ms/div]): DER with (a) current control and (b) VCL strategies for voltage-source NLL; DER with (c) current control and (d) VCL strategies for current-source NLL.

source NLL connection at the PCC. The VCL strategy reduced the PCC THD voltage from 2.18% to 1.41% compared to DER current control. Due to the selective virtual low-impedance paths for harmonics created by VCL strategy, the harmonic currents drained by the current-source NLL circulate between the DER arms, improving the THDi of the grid current from 17.9 to 5.89%. Comparing the PCC THDv after enabling HCC, the performance of the VCL

strategy is better when the voltage-source NLL is considered with respect to the current-source NLL. These results are in accordance with the analyses developed in Sections III and IV.

VI. CONCLUSIONS

This paper compared the performance of VDB-HCC strategies to mitigate the current harmonic content of different signatures of NLLs. VDB-HCC strategies operate satisfactorily under weak grid conditions (short circuit capacity of approximately 40 kVA), with high current-source and voltage-source NLL penetration. It was also demonstrated that VDB-HCC strategies are not suitable under stiff grid conditions, with high short circuit capacity. Frequency response analysis revealed better effectiveness of the VDB-HCC strategies for voltage-source NLLs, even with a more pronounced harmonic spectrum than current-source NLLs. In terms of selective HCC compensation performance, the VCL strategy shows better steady-state results in terms of THD grid current reduction compared to the SCL and DCL strategies, regardless of current-source or voltage-source NLL. Experimental results also showed better effectiveness of VCL in reducing PCC THD under weak grid conditions for voltage-source NLL compared to current-source NLL.

VII. AUTHOR CONTRIBUTIONS

CALLEGARI, J.M.S.: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Project Administration, Resources, Software, Validation, Writing – Original Draft. **BASTOS, R.R.**: Conceptualization, Formal Analysis, Funding Acquisition, Resources, Supervision, Visualization, Writing – Review & Editing. **CUPERTINO, A.F.**: Conceptualization, Formal Analysis, Funding Acquisition, Resources, Supervision, Visualization, Writing – Review & Editing. **BRANDÃO, D.I.**: Conceptualization, Formal Analysis, Funding Acquisition, Investigation, Resources, Supervision, Validation, Visualization, Writing – Review & Editing. **PEREIRA, H.A.**: Conceptualization, Formal Analysis, Funding Acquisition, Resources, Supervision, Validation, Visualization, Writing – Review & Editing.

PLAGIARISM POLICY

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