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Control Performance Assessment of a Zero Harmonic Distortion Grid-Forming Converter for Medium Voltage Islanded Microgrids

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ABSTRACT The world is currently witnessing a rapid transformation in the production and utilization of electrical energy. The traditional centralized generation model for electric power is swiftly evolving into a more decentralized system, known as Distributed Generation (DG), which incorporates renewable energy sources situated closer to end-users. This shift towards DG has paved the way for the emergence of grid-forming converters, which play a pivotal role in enhancing voltage and frequency stability within microgrids (MGs) and isolated applications. This study focuses on assessing the performance of the Zero Harmonic Distortion (ZHD) in both stand-alone and parallel operation modes. The distinctive feature of this converter lies in its inherent ability to generate a sinusoidal voltage source without the need for capacitive filtering components, which can adversely affect cost, efficiency, and size while potentially contributing to resonance problems. This is achieved through a judicious combination of harmonic cancellation within a three-winding transformer and the utilization of Selective Harmonic Elimination Pulse Width Modulation (SHE PWM) dismissing a closed-loop control structure. Simulation and hardware-in-the-loop results presented in this work demonstrate the satisfactory performance of the ZHD grid-forming converter.

KEYWORDS Distributed generation, grid-forming converters, AC microgrids, power systems, selective harmonic elimination, power converters.

I. INTRODUCTION

The electric power system is undergoing a significant transformation driven by the widespread adoption of distributed generation (DG). Environmental concerns, sustainability imperatives, and a growing demand for energy are collectively propelling the transition from conventional fossil fuel and nuclear-based power generation plants to renewable energy sources, particularly those interfaced with inverters, such as solar and wind energy [1]–[3].

In this context, DG emerges as a solution that makes a valuable contribution by bringing energy generation closer to consumers. This approach opens up opportunities for improved efficiency, investments, flexibility, stability, and power quality [4]–[6]. With the evolution of DG, the concept of the microgrid (MG) has also come into prominence. A microgrid is founded on a combination of loads, storage elements, and microsources, primarily relying on renewable energy sources such as solar, wind, and biomass [7].

The MG can operate in either connected or islanded modes. When connected to the main grid, both voltage and frequency are imposed by the utility system. However, in islanded mode, the MG operates independently, which imposes the presence of at least one grid-forming converter equipped with an energy storage system (ESS). This grid-forming converter, in conjunction with the ESS, assumes the pivotal role of establishing and maintaining the voltage and frequency within the MG. Alternatively, in scenarios with multiple grid-forming converters, they collectively coordinate power distribution based on their respective ratings and the availability of power from their associated energy sources [8], [9].

Particularly in islanded mode, power quality becomes a concern. Since the distributed energy resources (DERs) typically interface the point of common coupling (PCC) of the MG through LC or LCL switching harmonic filters, resonances points at various frequencies can arise. A variety of elements contribute to these complex resonance interactions within the MG, including passive filters, inductive line impedances, parasitic shunt capacitors, household capacitive-inductive loads, and disruptive loads exhibiting either constant voltage or constant power characteristics. The occurrence of these induced resonances can exert adverse effects on both transient and steady-state control performance, potentially leading to severe stability issues [10].

In literature a wide range of grid-forming converters applications is based on 2/3-level Voltage Source Converters (VSC) [11] and transformeless topologies such as Modular Multilevel Converters (MMC) [12]–[14]. In this context,

the ZHD converter proposed initially in [15] and [16] as a grid-feeding converter and latter in [17] as a grid-forming converter, shows advantages, as low parts count, simplicity of control and no need of output filters. The ZHD converter does not produce any characteristic harmonic until the 50^{th}, which is the maximum order considered in IEEE 519 and IEEE 1547 standards [18], [19]. This is achieved by employing two 3-phase converters, in 2 or 3-level topologies, using Selective Harmonic Elimination Pulse Width Modulation (SHE PWM) connected to a three-winding transformer, resulting in an inherently sinusoidal voltage source characteristic without the use of capacitive filtering elements that negatively impact in costs, efficiency, size, and complex resonances interactions issues.

The ZHD converter is a compelling alternative for operation as a grid-forming converter in MV MG applications such as university campuses, isolated communities and installations, military defense facilities and assets, and mission-critical microgrids [20]–[22] with simple control and consolidated technologies in the industry.

In this way, the main contribution of this work is to asses the ZHD grid-forming converter control performance sensitivity proposed in [17], in stand-alone and parallel modes.

The organization of this work is as follows: after the Introduction, section II presents the ZHD converter, its hardware, and control aspects. Sections III and IV shows the simulation and hardware-in-the-loop (HIL) results, respectively. Section V presents some conclusions.

A previous version of this work was presented in [23]. In the current version, the simulations was improved to characterize the converter working in medium voltage applications and hardware-in-the-loop results were included to demonstrate the ZHD control performance in the grid-forming mode.

II. ZERO HARMONIC DISTORTION GRID-FORMING CONVERTER

A. ZHD Converter

According to standards [18], [19], harmonics until the 50^{th} order are enough to characterize harmonic voltage and current distortion.

In this sense, a grid-forming converter that can deliver a voltage waveform free from harmonics until the 50^{th} order can be assumed as a sinusoidal voltage power source with zero harmonic distortion.

Fig. 1 shows the proposed ZHD converter. It consists of two 2-level VSCs connected to a three-winding transformer. The VSCs are connected in the star and delta secondaries. Due to the phase shift of 30 degrees between secondaries, it is expected a harmonic cancellation according to (1).

$$h = 6k \pm 1 \ \ \forall \ \ k \ odd \ and \ integer \tag{1}$$

In this context, it is possible to obtain a voltage waveform free from all the considered harmonics until the 50^{th} order,

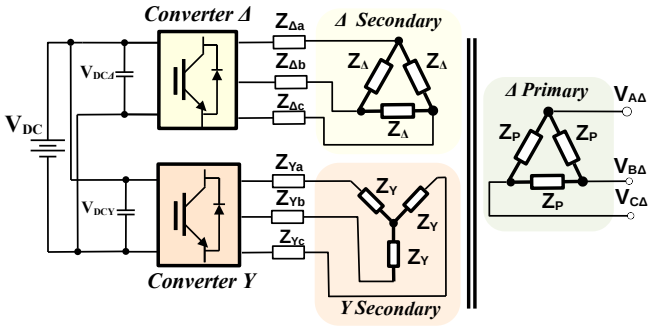

FIGURE 1. ZHD Grid-Forming converter.

by utilizing the SHE PWM technique to eliminate the harmonics not cancelled by the transformer. Table 1 shows the cancelled harmonics and the eliminated ones.

TABLE 1. ZHD Converter Harmonic Elimination and Cancellation.

Equipment	Harmonic Order
Transformer:	$5^{th}, 7^{th}, 17^{th}, 19^{th}, 29^{th}, 31^{th}, 41^{th}, 43^{th}, \ldots$
VSCs:	$11^{th}, 13^{th}, 23^{th}, 25^{th}, 35^{th}, 37^{th}, 47^{th}, 49^{th}$

B. Selective Harmonic Elimination

The SHE PWM is proposed in [24] and it is well established for two and three level converters applications. In [25], it is extended to cases where the fundamental amplitude control is required. Fig. 2 shows the voltage waveform generated in one phase of a two-level converter for a voltage modulation index m. The waveform is generated using the precalculus of switching angles $\alpha_1, \alpha_2, \alpha_3, \alpha_4, ..., \alpha_M$ related to the harmonics selected to be eliminated or mitigated, determining the number of switches in on period.

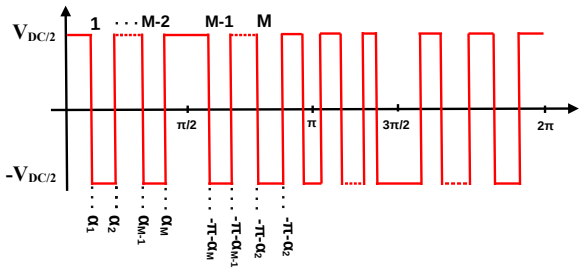

FIGURE 2. Generalized output voltage of 2L VSC.

The modulation index m is described by (2), where V_{1m} is the desired fundamental amplitude and $V_{1m6step}$ is the maximum fundamental voltage available, defined by (3). V_{dc} is the dc bus voltage [15].

$$m = \frac{v_{1m}}{V_{1ms6step}} \tag{2}$$

$$V_{1ms6step} = \frac{2 \cdot V_{dc}}{\pi} \tag{3}$$

The calculation of the switching angles as a function of the modulation index were performed offline using the Newton method and stored in Look-up Tables (LUTs), according to the numerical algorithm presented in [16]. A possible solution for commutation angles is shown in Fig. 3 as a function of the modulation index. These angles were chosen for the elimination of the harmonics listed in Table 1.

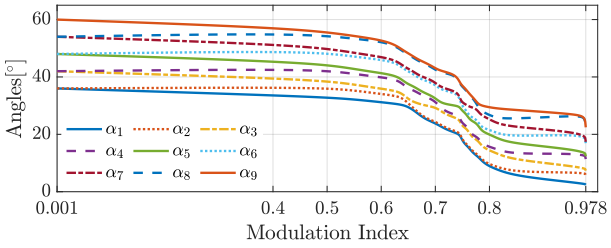

FIGURE 3. 2L VSC switching angles.

C. ZHD CONVERTER EQUIVALENT CIRCUIT MODEL

In this way, an analytical approach of the ZHD converter in grid-forming operation is proposed in [17] and it makes possible to obtain the per phase equivalent fundamental and harmonic circuits showed in Fig. 4.

These equivalent circuits reinforce the idea that no harmonic until the 50^{th} order is generated by the converter, delivering in practical terms, a sinusoidal voltage waveform. However, just like any other converter, if the MG demands harmonic currents, the PCC voltage waveforms are disturbed due to the voltage drop in the series impedance (4) of the converter (Fig. 4 (b)). $Z_{\Delta\phi}$ and $Z_{Y\phi}$ are the reactors impedances of the VSCs, Z_{Δ} and Z_Y are the impedances of the delta and wye secondaries, a is the transformer winding ratio and finally Z_P is the impedance of the primary winding.

$$Z_{ZHD} = (a^2(Z_{\Delta\phi} + \frac{Z_{\Delta}}{3})//a^2(Z_{Y\phi} + Z_Y)) + \frac{Z_P}{3} \tag{4}$$

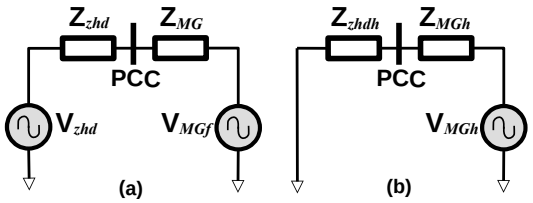

FIGURE 4. ZHD per phase: (a) fundamental equivalent circuit (b) harmonic equivalent circuit.

D. ZHD GRID-FORMING CONTROL STRUCTURE

Due to the inherent voltage source characteristic, the converter needs neither the voltage and current controls nor the ac voltage capacitors in voltage source operation.

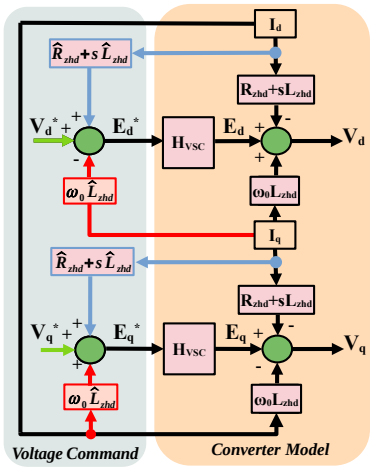

FIGURE 5. Voltage Command Control of ZHD Grid-Forming converter.

The voltage response in the dq frame is shown in (5). E_d and E_q are the synthesized voltages by the converter, and V_d, V_q, I_d, and I_q are the output voltages and currents, respectively. R_{zhd} and L_{zhd} are the output resistance and inductance of the converter impedance given by (4), and ω_0 is the fundamental frequency.

$$\begin{aligned} V_d &= E_d + \omega_0 L_{zhd} i_q - R_{zhd} i_d - L_{zhd} \frac{di_d}{dt} \\ V_q &= E_q - \omega_0 L_{zhd} i_d - R_{zhd} i_q - L_{zhd} \frac{di_q}{dt} \end{aligned} \tag{5}$$

The block diagram of the voltage command control is indicated in Fig. 5 and reveals that only a feed-forward disturbance command is responsible to reject the load variations (voltage drop on the ZHD series impedance), therefore compensating the voltage reference command V_d^* and V_q^* , as can be shown in (6). E_d^* and E_q^* represent the compensated voltage commands.

$$\begin{aligned} E_d^* &= V_d^* - \omega_0 \hat{L}_{zhd} i_q + \hat{R}_{zhd} i_d \\ E_q^* &= V_q^* + \omega_0 \hat{L}_{zhd} i_d + \hat{R}_{zhd} i_q \end{aligned} \tag{6}$$

The dynamic stiffness of the voltage command control is given by (7), where it is possible to observe that the disturbance rejection depends of the estimated inductance $\hat{Z}_{zhd}$, multiplied by the current sensor and VSC transfer functions, and its real value Z_{zhd}.

$$\left| \frac{I(s)}{V(s)} \right| = \frac{1}{\hat{Z}_{zhd} H_{VSC}(s) - Z_{zhd}} \tag{7}$$

Fig. 6 shows the full ZHD grid-forming control. The total measured output current in the synchronous rotating frame, I_d and I_q, generates a compensating signal that is added to V_d^* and V_q^*, generated by a isochronous control in case of stand-alone operation or droop control in the presence of other grid-forming converters [9]. Based on a virtual impedance concept, this structure allows the output voltage amplitude and phase compensation in the primary of the ZHD converter. $\hat{R}_{zhd}$ and $\hat{L}_{zhd}$ are the estimated

ZHD converter series resistance and inductance. There is also the possibility of current limitation in case of fault and of impedance emulation [12], [13].

Taking into account the transformer winding ratio a, E_d^* and E_q^* are used to calculate the modulation indexes $m_{\Delta,Y}$ and phase compensation $\delta_{\Delta,Y}$. The modulation signals and the sum of phase compensation and the angle references θ_Y and θ_Δ are compared in the LUTs generating the power switches command signals $\alpha_{1Y}, .., \alpha_{MY}$ and $\alpha_{1\Delta}, .., \alpha_{M\Delta}$.

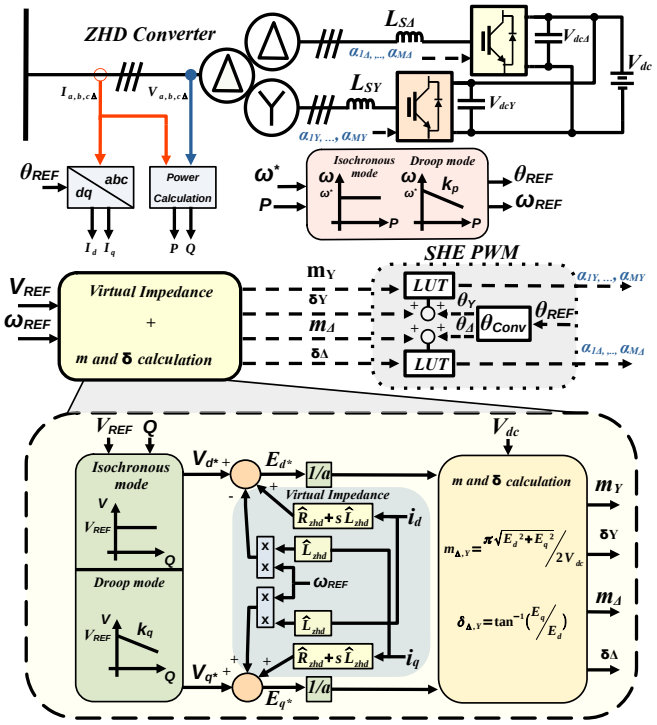

FIGURE 6. Control of ZHD Grid-Forming converter.

III. VOLTAGE CONTROL SIMULATION

A. Voltage and frequency regulation in stand-alone and parallel modes

The control performance of the ZHD grid-forming converter considering the stand-alone and parallel modes was analyzed based on typical load connection and disconnection scenarios. These scenarios consist in the connection or disconnection of loads with different characteristics: resistive, capacitive, inductive, nonlinear and DERs. Considering both operation modes, the ZHD converter was simulated in a microgrid using MATLAB/Simulink platform, as shown in Fig. 7. The system parameters are described in Table 2.

In a first moment, a period of simulation of 1.6s is adopted. In order to evaluate the ZHD voltage and its frequency regulation capacity, the connection of loads and of the DER are in this sequence:

- t = 0 s $\rightarrow$ (I) $\rightarrow$ S_1 is closed and ZHD_1 starts in isochronous mode and R load is connected ;

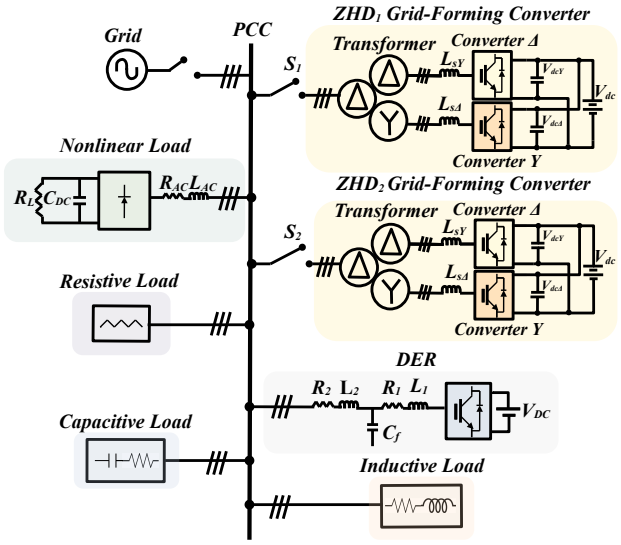

FIGURE 7. Islanded MG with ZHD Grid-Forming converter.

TABLE 2. Converter Data for Simulation Results

ZHD CONVERTER			
Parameters	**Values**	**Parameters**	**Values**
Rated Power	280 kVA	Frequency	60 Hz
Primary Voltage	13.8 kV	Δ and Y Secondary Voltages	440 V
$L_{\phi\Delta}$ and $L_{\phi Y}$ reactors	0.59/0.506 mH	DC link voltage	600 V
THREE-WINDING THREE-PHASE TRANSFORMER - Dd0y1			
Parameters	**Values**	**Parameters**	**Values**
R_m	526.7 $k\Omega$	$R_{s\Delta}$	19.4 $m\Omega$
L_m	534.5 H	$L_{s\Delta}$	3.33 μH
$R_{P\Delta}$	10.5 Ω	R_{sY}	16 $m\Omega$
$L_{P\Delta}$	108.7 mH	L_{sY}	84.26 μH
DER			
Parameters	**Values**	**Parameters**	**Values**
R_1	0.1 Ω	L_1 and L_2	500 μH
R_2	0.1 Ω	T_x	440 V/ 13.8 kV
C_f	110 μF	V_{DC}	800 V
LINEAR LOADS - R, RL and RC LOADS			
Parameters	**Values**	**Parameters**	**Values**
Active Power (P)	100kW	Reactive Power (Q)	0 var
Active Power (P)	40 kW	Reactive Power (Q)	30 kvar
Active Power (P)	40 kW	Reactive Power (Q)	-30 kvar
NONLINEAR LOAD			
Parameters	**Values**	**Parameters**	**Values**
R_{AC}	152.35 Ω	L_{AC}	2.2 μH
C_{dc}	2.59 μH	R_L	34.56 $k\Omega$

- t = 0.43 s $\rightarrow$ (II) $\rightarrow$ RL load is connected;
- t = 0.55 s $\rightarrow$ (III) $\rightarrow$ The DER is adjusted to 100 A;
- t = 0.7 s $\rightarrow$ (IV) $\rightarrow$ The RL load is disconnected;
- t = 0.75 s $\rightarrow$ (V) $\rightarrow$ RC load is connected;
- t = 0.85 s $\rightarrow$ (VI) $\rightarrow$ The RC load is disconnected;
- t = 0.9 s $\rightarrow$ (VII) $\rightarrow$ The nonlinear load is connected;
- t = 1 s $\rightarrow$ $(VIII)$ $\rightarrow$ The DER is adjusted to 0 A.
- t = 1.2 s $\rightarrow$ (IX) $\rightarrow$ S_2 is closed and both ZHD_1 and ZHD_2 starts in droop control mode ($k_p = 1.78x10^{-7}Hz/W$, $k_q = 6.415x10^{-5}V/Var$);
- t = 1.5 s $\rightarrow$ (X) $\rightarrow$ The nonlinear load is disconnected;

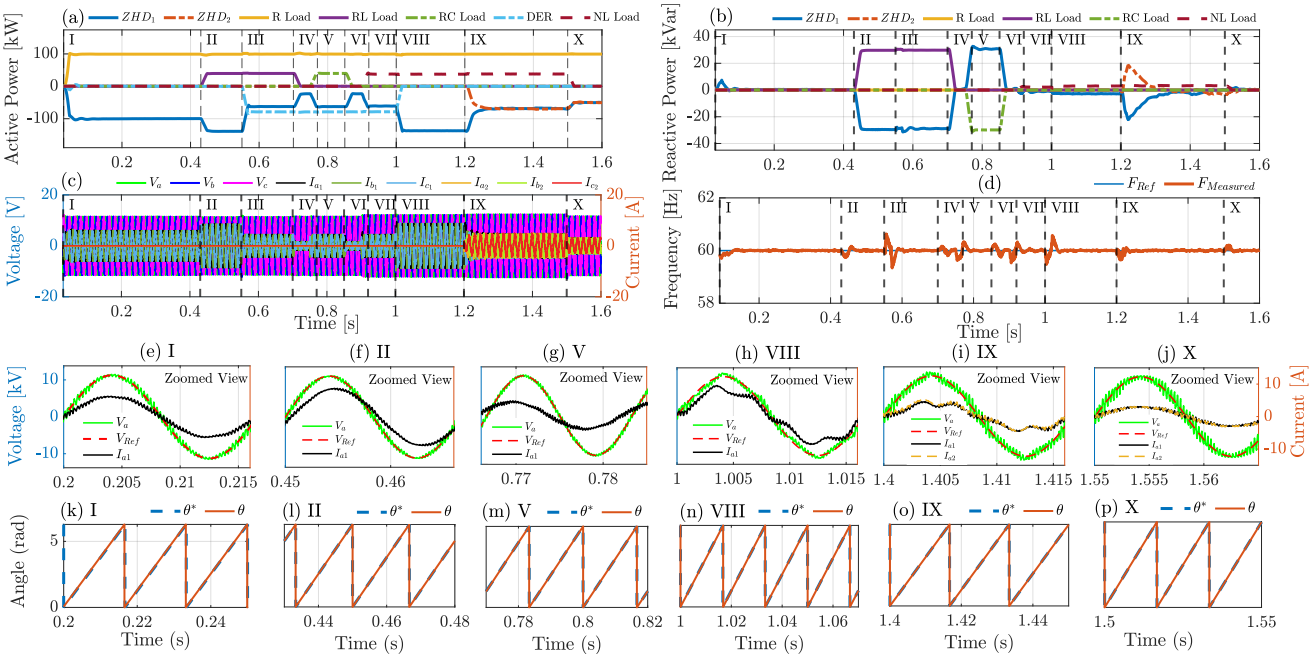

FIGURE 8. (a) Active power flow, (b) reactive power flow, (c) voltage at PCC and output currents at ZHD converters, (d) frequency at PCC, Zoomed view of phase A reference, measured voltage at PCC and current in ZHD converters in time instants: (e) I, (f) II, (g) V, (h) VIII, (i) IX, (j) X, reference and measured angle in time instants: (k) I, (l) II, (m) V, (n) VIII, (o) IX, (p) X.

Fig. 8 (a), (b), (c) and (d) shows active, reactive power flow, voltage at PCC and output currents at ZHD converters and frequency at PCC, respectively. It shows that the ZHD converter has the capacity of regulate the voltage and frequency at the PCC, always rejecting the disturbances and following the references. The zoomed view of I, II, V, VIII, IX and X simulation events can be observed in (e)-(p) and show that the converter can follow the voltage and angle references in case of resistive, inductive, capacitive and nonlinear loads and also can operates in parallel with other voltage controlled converters in power sharing mode.

Fig. 8 also shows the sinusoidal shape of the delivered voltage waveform in case of linear loads ((e), (f), (g) and (j)), and that the waveform is deteriorated in the presence of the nonlinear load ((h) and (i)).

Fig. 9 shows the phase A voltage FFT for each case. As can be expected, the delivered voltage waveform for linear loads is practically from from harmonics until the 50^{th} order ((a),(b), (c), (f)). However, when the nonlinear load is connected, the phase A voltage is disturbed by the demanded harmonic current. Fig. 9 (d) and (e) reveals the presence of harmonics not produced by the converter, but generated by the nonlinear load. Finally, Fig. 9 (g) and (h) shows the output current FFT showing both ZHD converters sharing the same fundamental and harmonic currents in case of nonlinear and linear load, respectivily.

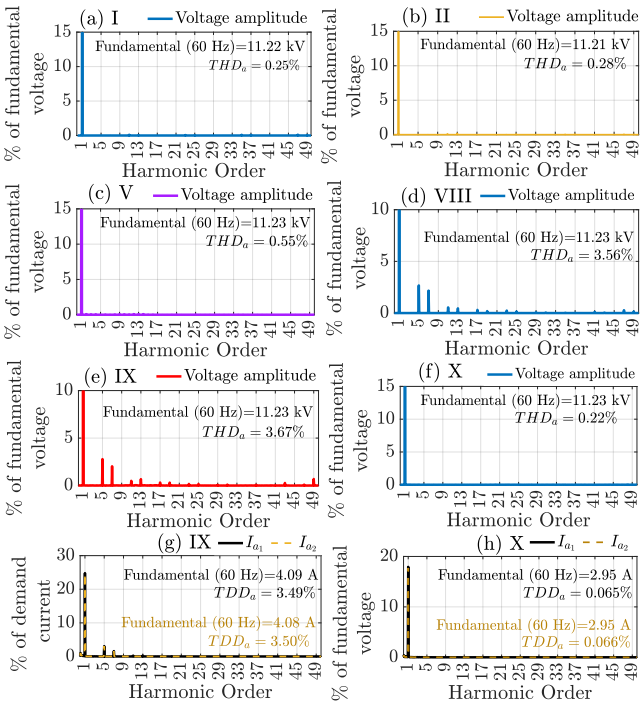

FIGURE 9. Output Voltage FFT for time events: (a) I, (b) II, (c) V, (d) VIII, (e) IX, (f) X, (g) IX and (h) X.

B. Sensitivity Analysis

Fig. 10 shows a important analysis regarding the dynamic stiffness of the command control shown in (7). The sensitivity analysis in the control system due to error in the converter estimated output impedance, for the same scenario of the last section, but considering cases with $\pm 20\%$ of estimating error in the ZHD_1 converter. Fig. 10 (a)-(d) show that the

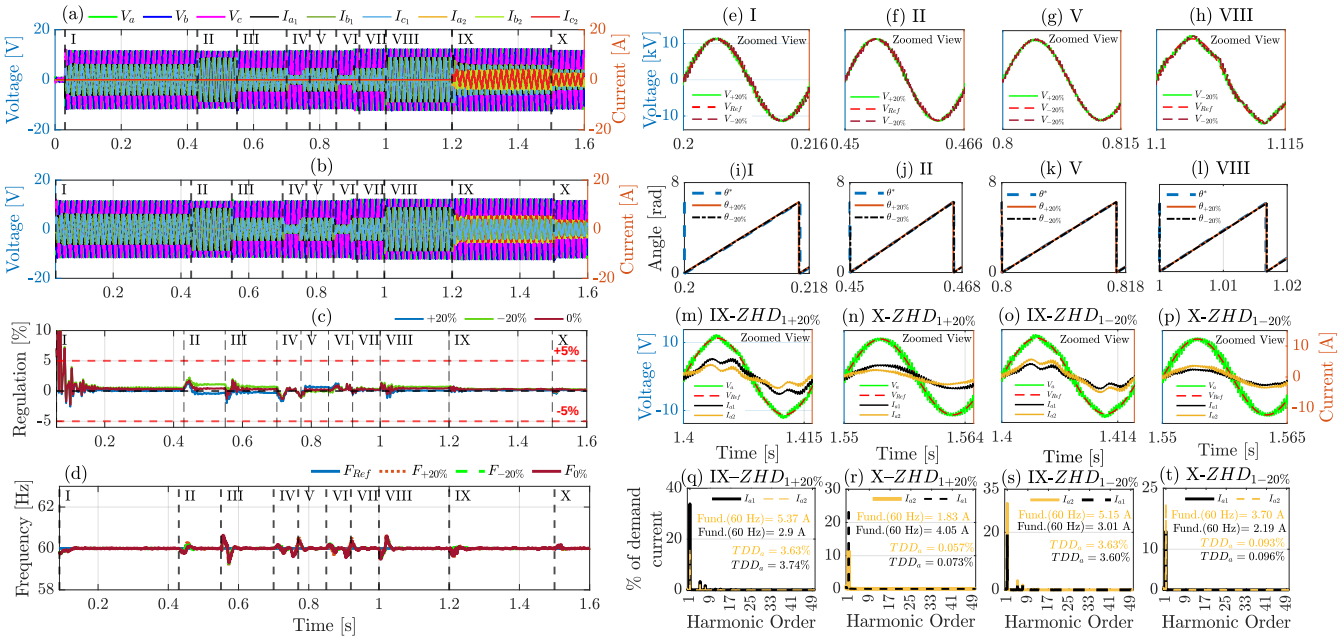

FIGURE 10. Considering estimating errors of $+20\%$ and -20% in ZHD_1 converter: a) Voltages at PCC and output currents at ZHD converters considering a error of (a) $+20\%$, (b) -20%, (c) PCC voltage regulation, (d) measured PCC frequency, zoomed view of phase A reference voltage and voltage at PCC in time instants: (e) I, (f) II, (g) V, (h) VIII, reference and measured angle in time instants: (i) I, (j) II, (k) V, (l) VIII, zoomed view of voltage at PCC and output currents at ZHD converters in time instants (m) IX, (n) X, (o) IX, (p) X, respectively, and output FFT voltage in time instants (q) IX, (r) X, (s) IX and (t) X.

converter can regulate voltage ((a),(b)) and frequency (d) with acceptable voltage regulation, as shown in (c), inside the $\pm 5\%$ limit recommend by standards [19], [26].

Considering the isochronous operation, Fig. 10 (e)-(l) clearly show that voltage and angle references could be tracked even considering the cases of $\pm 20\%$ of estimating error. However, the included estimating error causes a unequal current sharing between the both ZHD converters due to the differences in the virtual impedance between them. For the scenario shown in Fig. 10 (a), Fig. 10 (m) and (n) shows the phase A reference, measured voltage at PCC and the higher output current of ZHD_1 compared with ZHD_2 converter for time events IX and X. The FFT of the currents waveforms of (m) and (n) are shown in (q) and (r), respectively, reinforcing the differences between the currents.

The scenario shown in Fig. 10 (b) analogously shows the same effect, but with the ZHD_2 converter providing more current. For this case Fig. 10 (o) and (p) shows the phase A reference, the measured voltage at PCC and the output currents for both converters in time events IX and X. Fig. 10 (s) and (t) shows the FFT of the currents.

IV. HARDWARE-IN-THE-LOOP RESULTS

The ZHD converter was implemented on a real-time simulation platform to test and validate the ZHD control hardware. Figure 11 shows the actual controller connected to the HIL setup, where its steady-state and transient performance were thoroughly evaluated.

The ZHD controller rack contains a power supply board, a controller board (equipped with a Texas Instruments TMS320F28335 microcontroller) responsible for the voltage control, and an FPGA board (equipped with an FPGA model MAX 10 from Intel) that handles the SHE PWM operating at a sufficiently high sampling frequency (250 kHz) storing the switching angles (Table 3) with sufficient resolution.

One ZHD converter in the isochronous mode, was evaluated in three dynamics scenarios considering output impedance estimating errors of 0% , 20% and -20%, for a 50 kVA capacitive load (PF= 0.9), followed by a step load of 130 kW. Figs.12 to 14 show the results of each case followed by the zoomed views of phase A voltage and output current.

In all the cases, it is possible to verify the control structure voltage and frequency regulation capacity, rejecting the step load disturbance and as expected, delivering a practically sinusoidal voltage waveform. The voltage regulation also was evaluated, and even in the cases considering estimating error in the output impedance, the voltage regulation remains well below of 5%.

These results show that the ZHD converter is capable to operates as a grid-forming converter regulating voltage and frequency without capacitive filters, delivering sinusoidal voltage waveforms to an islanded MG only using a feed-forward disturbance command control.

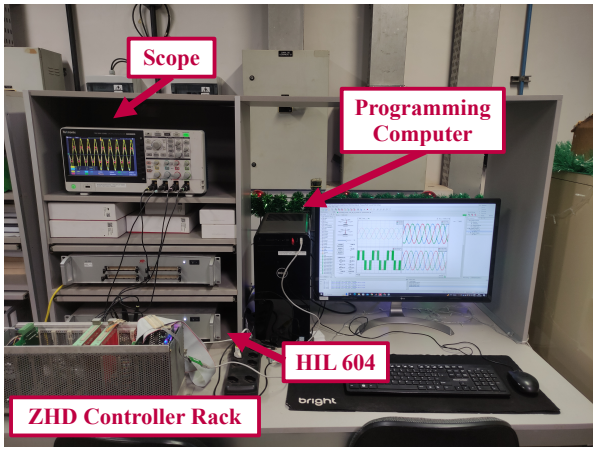

FIGURE 11. Structure of tests and validation in Hardware-in-the-Loop.

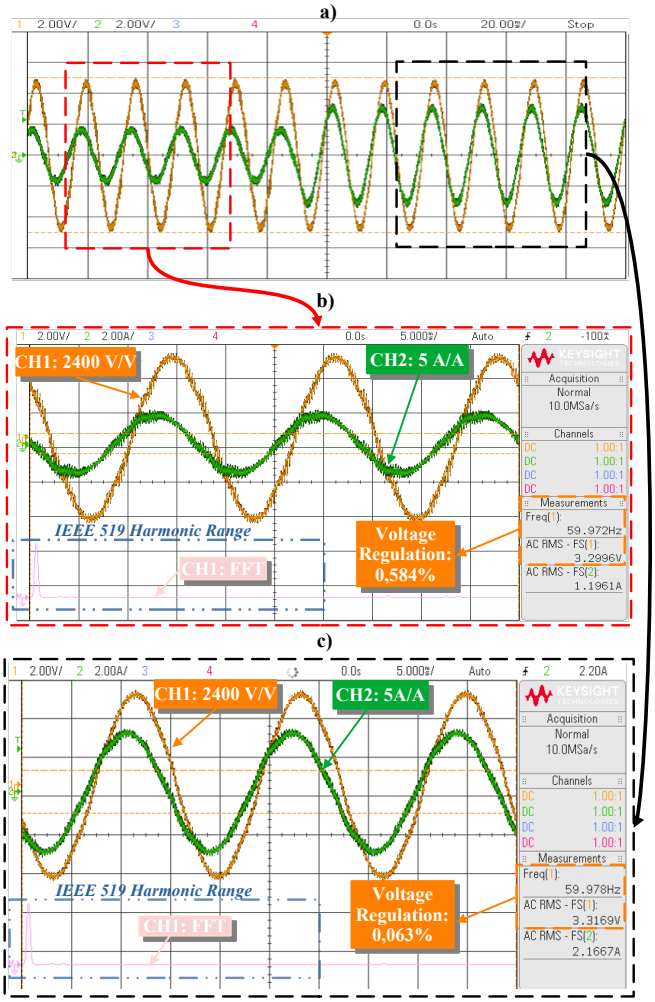

FIGURE 12. a) HIL results for a step load (phase A): PCC voltage (CH1), current (CH2) and FFT voltage (CH1) considering 0% of output impedance estimating error, b) Zoomed view before step load, c) Zoomed view after step load.

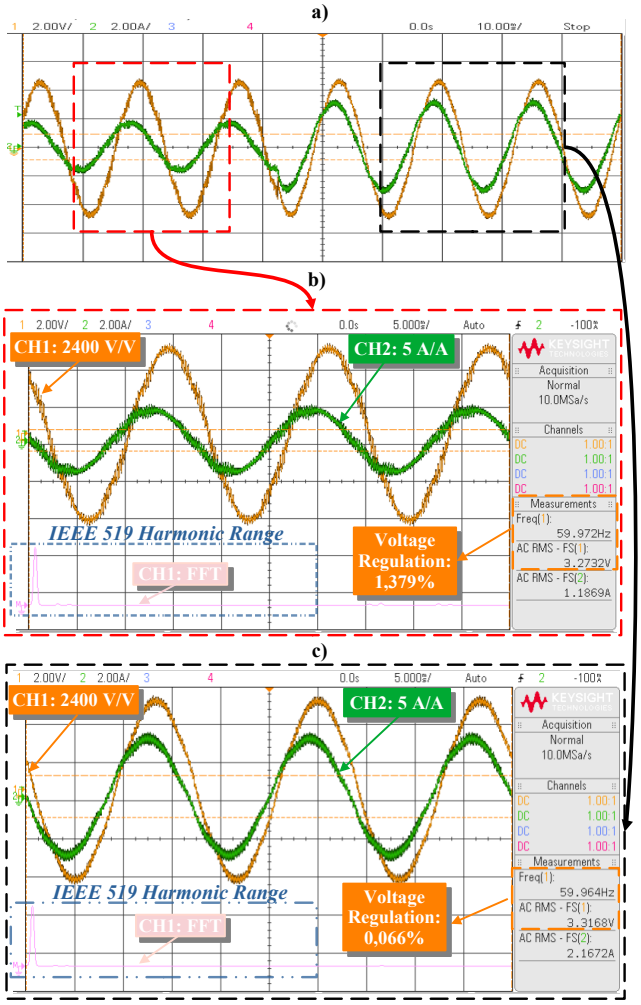

FIGURE 13. a) HIL results for a step load (phase A): PCC voltage (CH1), current (CH2) and FFT voltage (CH1) considering +20% of output impedance estimating error, b) Zoomed view before step load, c) Zoomed view after step load.

V. CONCLUSION

This paper has thoroughly evaluated the performance of the ZHD grid-forming converter control, demonstrating its robustness and efficacy in islanded microgrid (MG) applications. The control strategy, which includes feed-forward mechanisms to decouple disturbances, proved to meet current standards for both voltage regulation and harmonic content, even in the presence of series impedance estimation errors. Simulation results confirmed the converter's ability to effectively set and maintain voltage and frequency in both stand-alone and parallel modes, reinforcing its suitability for MG systems. Furthermore, hardware-in-the-loop testing, specifically in the isochronous mode, substantiated the converter's reliability and adaptability under real-world conditions. These results underscore the converter's potential for improving MG stability and resilience, offering a promising solution for future medium voltage microgrid applications.

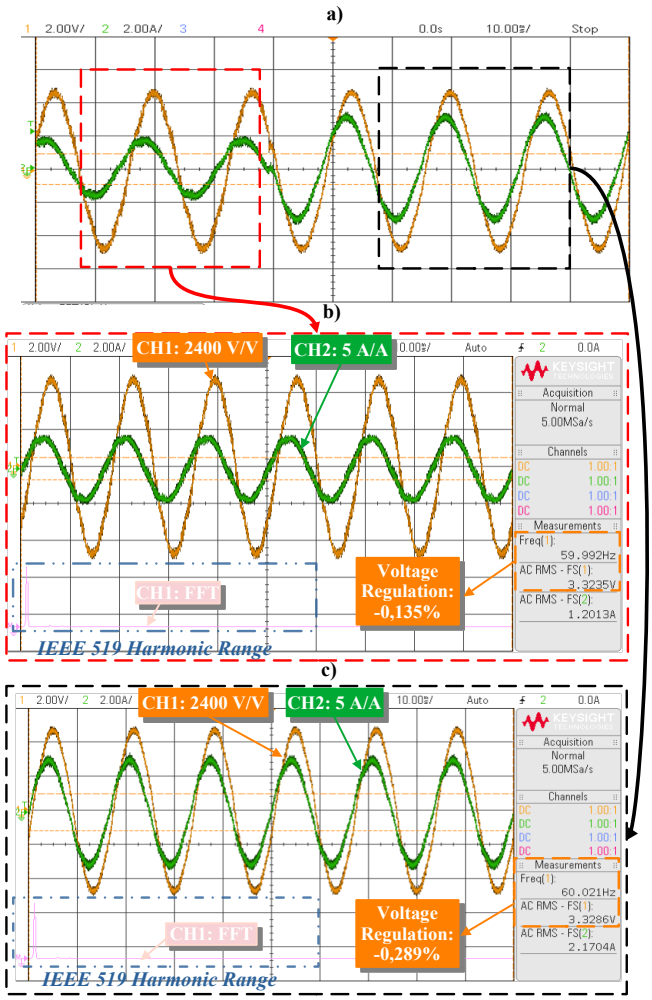

FIGURE 14. a) HIL results for a step load (phase A): PCC voltage (CH1), current (CH2) and FFT voltage (CH1) considering -20% of output impedance estimating error, b) Zoomed view before step load, c) Zoomed view after step load.

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AUTHOR'S CONTRIBUTIONS

RAMOS, G.V.: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **PARREIRAS, T.M.**: Conceptualization, Data Curation, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **CARDOSO FILHO, B.J.**: Conceptualization, Funding Acquisition, Project Administration, Resources, Supervision, Validation, Visualization.

PLAGIARISM POLICY

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