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Analysis of a MMC-Based 12 MW Direct-Drive Wind Energy Conversion System With Level-Shifted and Phase-Shifted PWM and Nearest-Level Modulation Strategies

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ABSTRACT This paper analyzes a 12 MW direct-drive wind energy converter system featuring a 6.6 kV, 132-pole permanent magnet synchronous generator, similar to the Haliade-X 12 MW manufactured by General Electric. The proposed system utilizes a back-to-back modular multilevel converter (B2B-MMC) with four submodules per arm. The research investigates three modulation strategies: nearest level modulation and two variants of multicarrier pulse width modulation that incorporate level-shift and phase-shift techniques. Additionally, it examines the interaction between the generator's low frequency and the design parameters of the MMC. Thus, this paper contributes to the understanding of the effectiveness of the B2B-MMC as a viable solution for direct-drive low-frequency wind generators. Furthermore, it analyzes how the modulation strategy and voltage equalization algorithm impact system performance, especially with the implementation of a subsampling technique. Digital simulations carried out with PSCAD/EMTDC provide a comparative analysis of the three modulation strategies investigated.

KEYWORDS Level-Shifted PWM, Modular Multilevel Converter, Nearest-Level Modulation, Phase-Shifted PWM, Wind Energy Conversion.

I. INTRODUCTION

In recent years, the growing concern about the environmental impact caused by fossil fuels has led to the search for renewable energy sources. In this scenario, wind energy stands out for its large generation capacity and for being competitive when compared to hydro and thermal sources. The wind farms can be build in land or offshore, being the second option advantageous in aspects such as: (*i*) wind speeds higher and more constant; (*ii*) larger areas available; and (*iii*) an easy logistical during the construction [1]. Due to these characteristics and a growing development of the wind energy conversion (WEC) systems, offshore applications can host high-power wind turbines.

Currently, there are wind turbines up to 14 MW available on the market, such as the SG14-222, manufactured by Siemens Gamesa, and the Haliade-X 14 MW, manufactured by General Electric. Reflecting the latest advances in the field, Ming Yang has announced plans to launch the MySE 16.0-242 wind turbine in 2024, boasting an impressive capacity of 16 MW. A recent review of multi-megawatt wind energy conversion systems enumerates the main characteristics of the newest commercial wind turbines [2]. An important issue with multi-MW WEC units is turbine/generator coupling. Although two-stage gearbox or medium-speed gearbox are commonly found in installations, direct drive for power ratings above 10 MW are offered by most manufacturers [3].

Two types generators are commonly used in WEC units: the Doubly-Fed Induction Generator (DFIG) and the Synchronous Generators (SGs), the latter including both wound rotor (WRSG) and permanent magnet (PMSG) designs. Recent studies have highlighted a growing preference for full-capacity back-to-back converters paired with PMSGs in multi-megawatt applications due to their reduced weight and volume [4]

There are also proposals in the literature to replace rare earth materials in PMSGs with high-temperature superconducting (HTS) coils [5]. However, a major challenge remains in addressing the low operating frequencies typical of direct-drive configurations. For instance, [6] and [7] propose permanent magnet synchronous generators (PMSGs) with capacities of 13.2MW / 3Hz and 12MW / 2Hz, respectively. Additionally, [4] introduces a 12MW / 10.45Hz WEC system featuring a PMSG with 132 poles, operating at 9.5 rpm.

In this context, selecting the optimal converter topology is essential to meet the power and voltage requirements

of modern systems. The primary options include: (*i*) using multiple two-level [8] or three-level [9] converters connected in parallel; (*ii*) adopting cascaded H-bridge (CHB) converters, which offer galvanic isolation through a medium-frequency transformer [10]; and (*iii*) implementing a modular multilevel converter (MMC) in a back-to-back configuration [11]. Each of these topologies presents unique advantages depending on the specific application needs.

The parallel configuration supports the use of low voltage generators, which insulation requirements are reduced. Although the higher generated current is shared between the parallel-connected converters, the harmonic content of the terminal voltages requires the connection of bulky passive filters, which represent a problem in installations with reduced space.

On the other hand, the CHB converter allows the use of medium-voltage generators, since the higher terminal voltage is divided across several series-connected units. In addition, the CHB converter can synthesize multilevel voltages, with lower harmonic content, simplifying the design of the output filters. Furthermore, because the generator current is reduced, the efficiency is improved due to lower joule losses. For more details on voltage and current levels, harmonic content, filter requirements, and related topics, please refer to [3] and [5].

Similar to the CHB converter, each phase of the MMC consists of multiple submodules connected in series. However, unlike the CHB, the converter legs are connected to a common DC link, making this topology well suited for back-to-back applications or a high-voltage direct current (HVDC) transmission systems, as originally proposed [12]. In addition to its capability to operate in high-voltage systems, as the DC bus voltage is distributed among the various series-connected submodules, the MMC can synthesize terminal voltages with multiple levels, simplifying harmonic filter design. However, in applications with variable frequencies, the voltage ripple in the capacitors of the MMC submodules may affect the converter's performance at low frequencies [13], [14].

Despite the aforementioned disadvantage, the use of MMCs with medium-voltage wind generators is being explored in the literature due to the converter's other advantages, including fewer semiconductor switches, reduced electrical losses, and lower harmonic content of the terminal voltages [15].

Fig. 1 shows a back-to-back (B2B) MMC topology, which has already been proposed for different configurations of WEC systems, for rated power from 1 MW to 10 MW [16], [17]. Reference [11] investigates the performance of a 5 MW B2B-MMC with a different number of half- and full-bridge submodules per converter arm. In all the aforementioned works, high-frequency sinusoidal pulse width modulation (PWM) schemes are employed to synthesize AC voltages with $(N+1)$ and $(2N+1)$ levels, where N represents the number of submodules per converter arm. However, high-frequency PWM strategies are not suitable for application in high-power converters, due to the voltages that must be blocked and currents that must be interrupted by the power semiconductor switches.

Motivation and contribution of the work

Building on the foundations laid out in [18], this work explores the implementation of a 12 MW direct-drive wind energy conversion (WEC) system. It closely examines a configuration consisting of a 6.6 kV/132-pole permanent magnet synchronous generator (PMSG), similar to General Electric's 12MW Haliade-X model [2] , integrated with a back-to-back modular multilevel converter (B2B-MMC) comprising four submodules per arm.

The research focuses on investigating the effect of the sampling period on the voltage equalization of the MMC submodules. Futhermore, three modulation strategies are tested: nearest level modulation (NLM) and two variants of multicarrier pulse width modulation (PWM) incorporating level shift (LS) and phase shift (PS) schemes [19]. Special attention is devoted to elucidating how the voltage equalization algorithm impacts the submodule switching frequency, with particular focus on exploring a subsampling technique [20].

Additionally, this work aims to clarify how the low generator frequency impacts the design of B2B-MMC parameters, such as submodule capacitance, arm inductance, and the filters required to interconnect the WEC unit with the grid. Through digital simulations conducted in PSCAD/EMTDC, the research provides a comparative analysis of three modulation strategies with varying sampling periods in the voltage equalization algorithm. Furthermore, it highlights the effectiveness of the B2B-MMC configuration as a viable solution for direct-drive, low-frequency wind generators.

Therefore, the main contributions of this paper are listed below:

- A comprehensive investigation of the performance of the B2B-MMC when it is applied to a direct-drive 12 kV wind energy converter (WEC) system;
- An analysis of how the voltage equalization algorithm and different modulation strategies affect the performance of the MMC-based WEC system;
- A discussion on the impact of a subsampling technique used in conjunction with the voltage equalization algorithm.

The rest of this paper is organized as follows: Section II shows and explains the parts of the proposed system, as well as all the controllers used; Section III presents the voltage equalization algorithm, the modulation strategies investigated and their effects in the switching stress; Section IV presents the methodology used to design the MMC parameters, as well as how the low operating frequency of the generator impacts them; Section V presents and discusses the results obtained with the digital simulation of the proposed system; finally, Section VI presents the conclusions of this work.

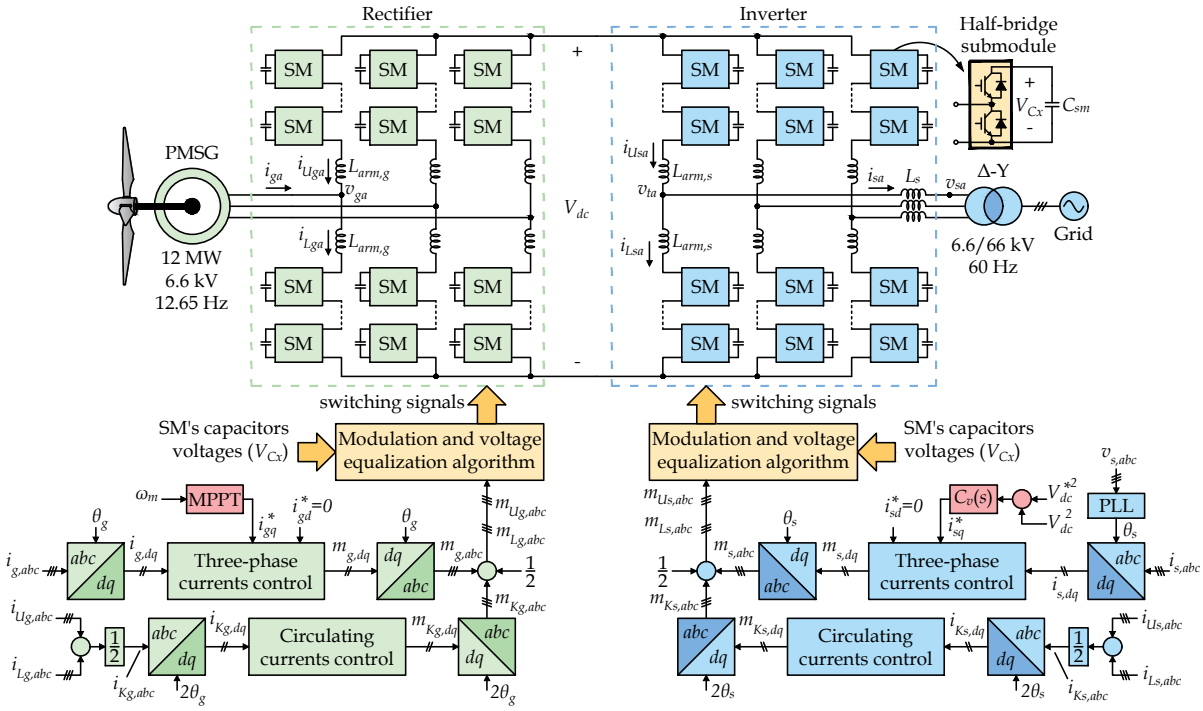


FIGURE 1. Schematic of the proposed WEC system with a B2B-MMC and the controllers used for both converters.

II. THE MMC-BASED WEC SYSTEM AND ITS CONTROLLERS

Fig. 1 shows a schematic diagram of the proposed WEC system, using a B2B-MMC with half-bridge submodules (SM). The half-bridge topology leads to the minimum number of switches, compared to other topologies as full-bridge and single-clamped submodule [21]. In this paper, four submodules per arm were used, this is, eight submodules per phase. Nowadays, the IGBT with the highest voltage is a 6.5 kV device, such as the FZ750R65KE3 manufactured by Infineon, for example. Considering a DC bus voltage of 13 kV, 20% above the peak-to-peak voltage of the 6.6 kV generator, each submodule must handle 3.25 kV, which is half of the capacity of the 6.5 kV IGBT.

The currents synthesized by both the rectifier and inverter converters are controlled in the *dq* reference frame [22]. An encoder measures the generator rotor angle θ_g, while at the grid side the angle θ_s is tracked by a phase-locked loop (PLL) circuit. The *d*-axis current reference is kept zero in both converters, while the *q*-axis current reference is generated by two different algorithms. On the rectifier side, the *q*-axis current reference is generated by a maximum power point (MPP) algorithm, which employs an optimal torque control (OTC) technique to extract maximum power from the generator [1]. On the inverter side, the controller $C_v(s)$ generates the *q*-axis current reference to regulate the DC link voltage.

Additional control loops, in the *dq* reference frame, were implemented in both converters to suppress circulating currents in the MMC arms, which primarily consist of even-order harmonics [23]. These controllers are specifically tailored to compensate for the second harmonic, as higher-order harmonics are negligible. To achieve this, the *dq* frame transformation operates at twice the fundamental frequency, enabling the system to isolate and process only the second harmonic component [24].

Finally, the reference signals for the arm voltages are sent to the modulation and voltage equalization block. Additionally, the rectifier and inverter controllers must be designed with consideration for the specific operating frequencies on both sides of the B2B-MMC. The mathematical modeling of the MMC is detailed in [20], while the modeling of the WEC system, with a permanent magnet synchronous generator (PMSG) is presented in [1]. The control system shown in Fig. 1 is versatile and can be applied to any modulation strategy and voltage equalization algorithm, which will be discussed in the following sections.

III. VOLTAGE EQUALIZATION ALGORITHM AND MODULATION STRATEGIES

Fig. 2 illustrates the flowchart of the voltage equalization algorithm. By comparing the reference signal with multiple carriers, the algorithm determines how many submodules need to be inserted or bypassed to achieve the desired voltage at any given moment.

The next step involves selecting specific submodules based on the direction of current flow through the MMC arm to keep the capacitor voltages balanced. If the arm current is positive, submodules with lower DC capacitor voltages

are inserted. Conversely, if the arm current is negative, submodules with higher DC capacitor voltages are selected.

This process relies on a selection and sorting algorithm that arranges the submodules according to their DC capacitor voltages. Further details about this selection and sorting algorithm can be found in [20].

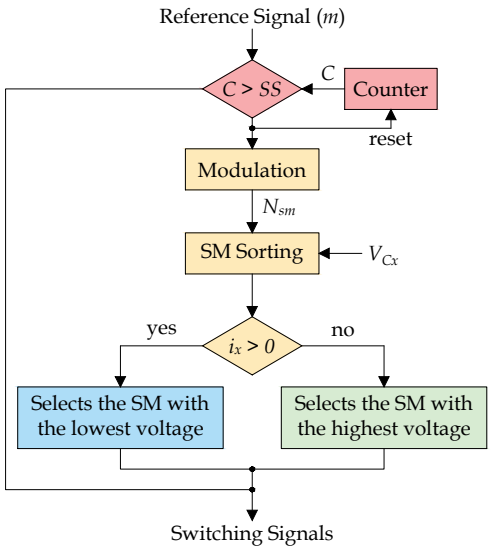


FIGURE 2. Flowchart of the submodules DC voltage equalization algorithm.

As the number of submodules increases, the computational effort required to sort them based on their DC voltages can become significant. To address this, a subsampling loop can be incorporated into the flowchart shown in Fig. 2. This adjustment ensures that the sorting algorithm is executed only when the counter (C) exceeds the subsampling multiplier (SS), thus reducing the computational burden.

In addition, different modulation strategies can be used to determine the number of submodules that will be inserted (N_{sm}). Fig. 3 illustrates the waveforms of the NLM strategy. In Fig. 3(a), a sinusoidal reference signal is compared to predefined voltage levels to determine the number of submodules (N_{sm}) that should be inserted at each moment. Fig. 3(b) shows how N_{sm} is adjusted based on these comparisons. The NLM strategy produces AC voltages with harmonics at low frequencies, such as 5th, 7th, etc. In the example shown in Fig. 3, the voltage levels are evenly spaced. However, these levels can also be adjusted to minimize or compensate for some specific harmonics [25]. Although this subject was not implemented in this work, the harmonic content of the voltages and currents may be reduced using passive filters.

Fig. 4 shows the waveforms of the LS-PWM strategy. In Fig. 4(a), the sinusoidal reference signal is compared to four triangular carriers, with the DC level shifted equally, to determine the number of submodules (N_{sm}) that should be inserted at each moment. Fig. 4(b) shows how N_{sm} is adjusted based on these comparisons. Despite the increase in the number of switches, the magnitude of the terminal voltage harmonics reduces with the increase in the number of carriers, making them easier to filter [26]. Additionally, it is very simple to add triangular carriers in this strategy when extra submodules are included in the converter structure, thereby reducing computational effort.

Fig. 5 depicts the waveforms of the PS-PWM strategy. In Fig. 5(a), the sinusoidal reference signal is compared to four phase-shifted triangular carriers, to determine the number of submodules (N_{sm}) that should be inserted at each moment. Fig. 5(b) shows how N_{sm} is adjusted based on these comparisons. Note that PS-PWM results in a higher number of commutations per cycle even when the phase-shifted triangular carriers have a frequency less than half the LS-PWM carrier frequency.

However, the phase shift of the triangular carriers positively impacts the equivalent switching frequency of the converter. Its frequency is multiplied by the number of carriers (or submodules), resulting in a decrease in the amplitude of the harmonics and a greater separation from the fundamental component, making them easier to filter [27]. Although this may lead to simpler filters, the computational effort may be larger, because a smaller sampling period is required for the microcontrollers for a same carrier frequency.

Comparing Fig. 3(b), Fig. 4(b) and Fig. 5(b) one can observe the increase in the number of commutations per cycle for each scheme, i.e. NLM, LS-PWM and PS-PWM, respectively. Nevertheless, the equalization algorithm increases the number of commutations per cycle, regardless of the modulation strategy, to maintain balanced the voltages of the submodules capacitors.

Fig. 6(a) shows the NLM switching pattern for an MMC with four submodules per arm, operating without an equalization algorithm, but with individual voltage regulation in the submodules. In this example, each submodule is inserted and bypassed only once per cycle.

Fig. 6(b) shows the NLM switching pattern for an MMC with four submodules per arm, operating with the equalization algorithm, but without subsampling. It was used a 60 Hz sinusoidal reference and a sampling period of 10 µs. Note that, due to the equalization algorithm, there is a high number of commutations, except during periods when all submodules are simultaneously inserted or bypassed.

By enabling subsampling in the equalization algorithm (Fig. 2), the number of commutations per cycle can be reduced. Fig. 6(c) and Fig. 6(d) show the NLM switching pattern for an MMC with four submodules per arm, operating with the equalization algorithm and a subsampling ratio of 10 and 20 times, respectively. Considering the sampling period of 10 µs, the equalization algorithm will run every 100 µs and 200 µs, respectively. It will be shown in the simulation results section that, despite reducing the number of commutations per cycle, the subsampling technique can impact the quality of the voltages and currents synthesized by the MMC.

A behavior similar to that shown in Fig. 6 can be observed when using the LS-PWM and PS-PWM strategies. However,

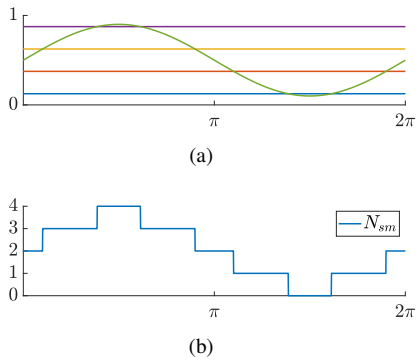


FIGURE 3. NLM: (a) comparison between levels and reference; (b) number of submodules to be activated.

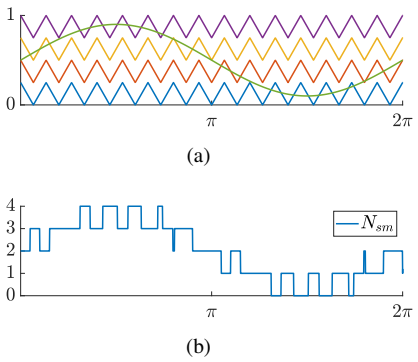


FIGURE 4. LS-PWM: (a) comparison between triangular carriers and reference; (b) number of submodules to be activated.

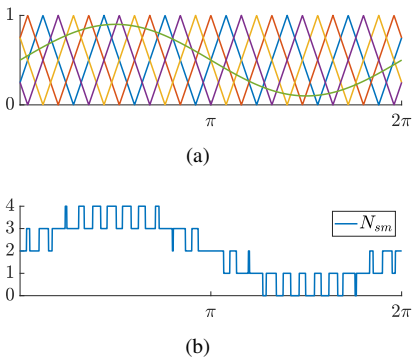
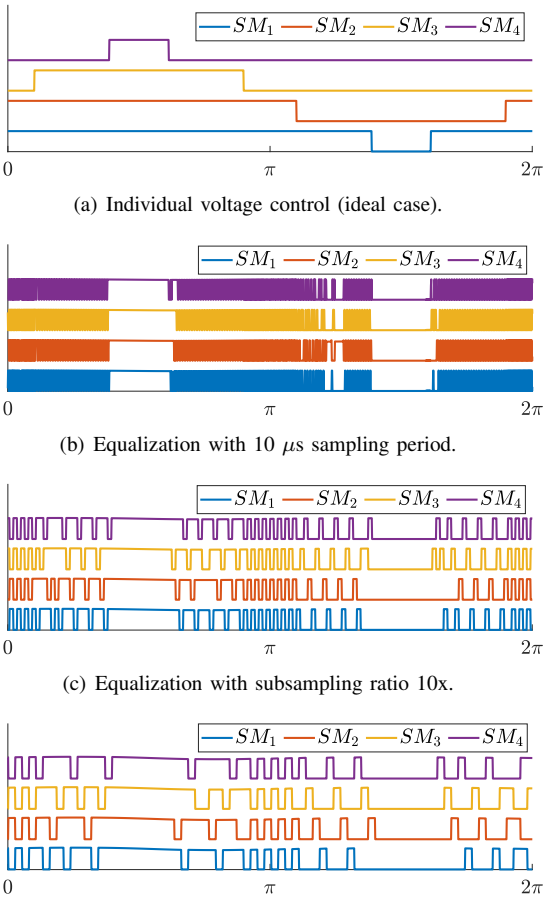


FIGURE 5. PS-PWM: (a) comparison between triangular carriers and reference; (b) number of submodules to be activated.



(a) Individual voltage control (ideal case).

(b) Equalization with 10 μs sampling period.

(c) Equalization with subsampling ratio 10x.

(d) Equalization with subsampling ratio 20x.

FIGURE 6. NLM switching pattern for an MMC with four submodules per arm, incorporating individual voltage control, voltage equalization algorithm, and subsampling technique.

under ideal conditions with the equalization algorithm disabled, the switching frequency of all semiconductor devices in the PS-PWM technique matches the triangular carrier frequency. In contrast, this relationship does not hold for the LS-PWM strategy, where semiconductor devices experience unequal switching frequencies and conduction times. This imbalance requires the use of rotation techniques to evenly distribute switching and conduction losses across the submodules. In addition, the waveforms synthesized using the LS-PWM strategy exhibit a lower THD compared to those produced by the PS-PWM technique, particularly when the amplitude of the synthesized voltage is lower than the maximum [28].

Conversely, when the equalization algorithm is enabled, the number of commutations per cycle becomes very similar across all modulation strategies. Therefore, one can conclude that when utilizing the equalization algorithm, the average switching frequency of the submodules is primarily determined by the sampling frequency of the algorithm rather than the frequency of the triangular carriers.

Table 1 summarizes the number of commutations per cycle for the three modulation strategies investigated, i.e. NLM, LS-PWM and PS-PWM. This analysis is based on a 60 Hz sinusoidal reference signal and includes individual voltage control, a voltage equalization algorithm, and the subsampling technique, as illustrated in Fig. 6. Only the rising edge, indicating when the submodule was inserted, was counted. The LS-PWM and PS-PWM techniques were simulated with carrier frequencies of 1500 Hz and 375 Hz, respectively.Despite the higher number of commutations typically anticipated for the PS-PWM technique, the total number of commutations is quite similar, for all strategies, when the equalization algorithm and subsampling technique are employed.

TABLE 1. Average number of commutations of a submodule in a period of a sinusoidal reference of 60 Hz.

Modulation	Subsampling			
	Ideal	1x	10x	20x
NLM	1	129	32	17
LS-PWM	4	127	31	17
PS-PWM	6	126	31	18

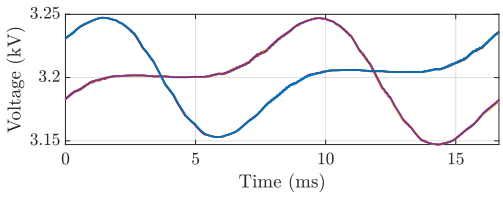
According to [29], the switching losses for the submodule semiconductors increase linearly with switching frequency, and the average commutation power loss is calculated as

follows:

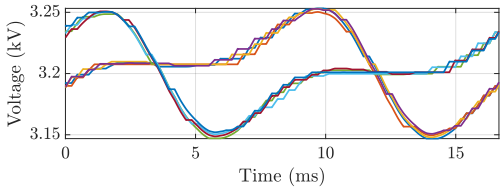
$$P_{sw} = \frac{1}{2} V_{Cx} I_{arm} f_{sw} (t_{on} + t_{off}), \tag{1}$$

where P_{sw} is the average switching power loss, V_{Cx} is the submodule capacitor voltage, I_{arm} is the arm current, f_{sw} is the average switching frequency, t_{on} and t_{off} are the turn-on and turn-off time, respectively.

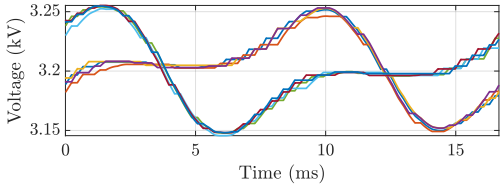
In order to evaluate the impact of the sampling period and triangular carrier frequency on the performance of the equalization algorithm for regulating DC capacitor voltages at 3.2 kV, an MMC, with four submodules per arm, was simulated using LS-PWM with a time step of 10 µs. Fig. 7(a) shows the voltages of the submodules capacitors considering 1x subsampling and a triangular carrier frequency equal to 1260 Hz. Note that that the average values of the DC voltages across the submodules are nearly equal. Fig. 7(b) illustrates the DC voltages of the submodules when the subsampling rate is increased by 20x and the triangular carrier frequency is kept the same as in the previous case. Note that the DC voltages remain equalized, although the waveforms are slightly degraded. Finally, Fig. 7(c) depicts the DC voltages of the submodules when the triangular carrier frequency is increased to 12.6 kHz while the subsampling rate is kept the same as in the previous case. Note that increasing the triangular carrier frequency has a small influence on the performance of the equalization algorithm.



(a) Carriers of 1260 Hz and 1x subsampling.



(b) Carriers of 1260 Hz and 20x subsampling.



(c) Carriers of 12.6 kHz and 20x subsampling.

FIGURE 7. Voltages of the submodules capacitors using LS-PWM with the voltage equalization algorithm.

Regardless of the modulation strategy and subsampling rate used, the MMC parameters must be designed following technical criteria, as will be discussed below.

IV. DESIGN OF THE MMC PARAMETERS

The submodule capacitance should be designed to minimize voltage ripple, while the arm inductance should be chosen to prevent resonance with high-order harmonics. Additionally, the output interface (RL) filter must be designed to comply with grid-code requirements regarding total harmonic distortion (THD) for the collector grid [30]. This paper will focus specifically on the design of the submodule capacitance and arm inductance, as they are influenced by the low frequency of the generator.

According to the method proposed in [31], the MMC submodule capacitance C_{sm} can be calculated as follows:

$$C_{sm} = H \left(\frac{N}{3} \frac{S_{mmc}}{V_{dc}^2} \right), \tag{2}$$

where N is the number of converter arm submodules, S_{mmc} is the converter rated power, V_{dc} the DC bus voltage, and $H = (\varepsilon\omega)^{-1}$ is the equivalent capacity discharging time constant, being ω is the AC system frequency and ε the maximum voltage ripple rate for the submodules DC capacitors.

Based on (2), to calculate the submodule capacitance, it is essential to consider the grid frequency ω and determine the maximum allowable DC voltage ripple rate ε. Note that as the frequency ω decreases, the corresponding value of H increases. This behavior is also observed with the ripple ε. In the case of a low-frequency generator, a large value of H will require a very high capacitance C_{sm} in the submodules, which may make the use of a B2B-MMC with PMSG operating at 2 and 3 Hz impractical.

In addition to addressing the maximum voltage ripple, it is essential to ensure voltage stability in the DC link connecting the two MMC converters [14]. When considering the same voltage fluctuation ε for both converters, the capacitance of the inverter submodules will be smaller because the grid frequency is higher than the generator frequency. However, if the two converters have different discharge time constants H, this can lead to unstable operation. To prevent this issue, the capacitance should be designed based on the lower frequency side converter, while maintaining the time constant H for the higher frequency side.

The arm inductance can be designed based on the resonant frequency of the MMC arm's equivalent impedance. This resonant frequency should be set at twice the AC system frequency to avoid resonance with higher-order harmonics, allowing the arm inductance to be calculated as follows:

$$L_{arm} = \frac{N}{C_{sm}(2\omega_s)^2}, \tag{3}$$

where N is the number of submodules per arm, C_{sm} is the submodule capacitance and ω_s is the angular frequency of the grid.

From (3), it can be concluded that low frequencies will require large arm inductance. This characteristic may be another practical problem for MMC-based rectifiers interfacing with low-frequency generators.

The next section presents simulation results for a direct-drive PMSG WEC system based on B2B-MMC, designed according to the methodologies described in the previous sections.

V. SIMULATION RESULTS

The configuration depicted in Fig. 1 was modeled and simulated using PSCAD/EMTDC. Each three-phase MMC was configured with four submodules per arm, while the DC bus voltage was set at 13 kV. The components of the MMC and the controller parameters were designed uniformly across all modulation strategies to ensure a fair comparison under the same conditions. A maximum DC voltage ripple ratio of 10% was considered for the design of the MMC-based rectifier. Table 2 and Table 3 summarize the main parameters of the PMSG wind generator and the B2B-MMC, respectively.

TABLE 2. Main parameters of PMSG wind generator.

Parameter	Value
Generator rated power	12 MW
Rated voltage of the generator	6.6 kV
Number of poles of the generator	132
Rated frequency of the generator	12.65 Hz
Generator resistance	72.6 mΩ
Generator inductance	5.6 mH

TABLE 3. Main parameters of B2B-MMC.

Parameter	Value
Rectifier arm inductance	20 mH
Rectifier arm resistance	50 mΩ
B2B DC bus voltage	13 kV
Submodules capacitance	12 mF
Inverter arm inductance	2 mH
Inverter arm resistance	30 mΩ
Grid filter inductance	2 mH
Grid filter resistance	20 mΩ
Grid rated frequency	60 Hz
Grid transformer voltage ratio	6.6/66 kV

The NLM, with the voltage levels evenly spaced, the LS-PWM and the PS-PWM, with 1260 Hz triangular carriers, strategies were used to synthesize terminal phase voltages with (N+1) levels.

Despite the three-phase configuration of the B2B-MMC, each submodule, based on half-bridge converter, operates as a single-phase unit. Therefore, when selecting the triangular carrier frequencies for the LS- and PS-PWM schemes, various practical considerations must be taken into account.

Thus, considering a bipolar switching strategy to control the half-bridge submodule, harmonic voltages will appear in side-bands centered at the frequencies $(n\omega_c \pm m\omega)$, where ω_c and ω represent the angular frequencies of the triangular carrier and the fundamental output voltage, respectively. For odd values of n there are only harmonics for even m; and for even values of n, there are only harmonics for odd m. Therefore, to prevent overlap between the harmonic at $(\omega_c - 2\omega)$ and the fundamental component, ω_c must be selected to be greater than (3ω). Similarly, to prevent overlap between the harmonics at $(2\omega_c - 3\omega)$ and $(\omega_c + 2\omega)$, $\omega_c > (5\omega)$ [32].

In addition, according to [29], to eliminate even harmonics in the terminal voltages and prevent unwanted sub-harmonics in the output voltages, the carrier waveform should be synchronized, with its frequency being an odd integer multiple of the reference voltage's fundamental frequency. However, if the carrier frequency is at least 21x higher than the fundamental frequency, the sub-harmonics resulting from asynchronous PWM become negligible and can be ignored.

As shown in Section III, the submodules switching frequency is manly influenced by the subsampling period. As expected for any electronic converter, the harmonic distortion may be reduced using higher frequencies for the triangular carrier. However, due to the voltage equalization algorithm and subsampling technique, the carrier frequency has no significant impact on the switching stress of the semiconductor switches. Therefore, only the results for the minimum frequency modulation ratio 21x will be shown ahead.

A. Wind Speed Variation

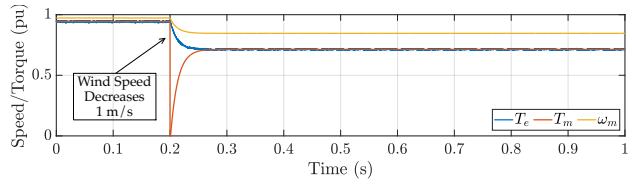
In the first test, the PMSG operates at rated conditions, with wind speed of $12.3\ \mathrm{m/s}$, when in $t = 0.2$ s the wind speed is step-reduced in $1\ \mathrm{m/s}$. This test aims to verify the dynamic stability of the WEC unit with the proposed control strategy. All modulation strategies were tested, with 1 µs time step and subsampling ratios of 1x, 10x, 100x and 200x. However, due to the lack of space, only the results of LS-PWM with 10x subsampling are shown in Fig. 8 and Fig. 9. A steady-state analysis of the three-phase currents is presented further, in Fig. 10, Fig. 11 and Fig. 12.

Fig. 8(a) shows the electromagnetic and mechanical torques along with the angular speed of the turbine/generator shaft, all in pu. The WEC unit starts operating with rated angular speed, when in $t = 0.2$ s, when the wind speed is step-reduced. Since the mechanical torque provided by the wind turbine is reduced, the electromagnetic torque is adjusted and the angular speed is reduced by the MPPT, in order to keep tracking the maximum power.

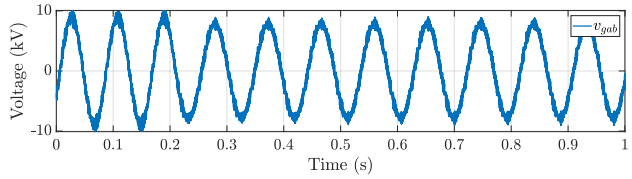
Fig. 8(b) and Fig. 8(c) show the terminal line voltage and the three-phase currents of the rectifier, respectively. After the wind speed reduction in $t = 0.2$ s, the line voltage and the currents are reduced as well. The large arm inductors filter the terminal voltages, therefore the levels are not evident in the line voltage v_{gab}, which is very close to a sinusoidal waveform. The filtered terminal voltages and the inductance

of the generator lead to currents with an almost sinusoidal waveform, even for a 10x subsampling ratio.

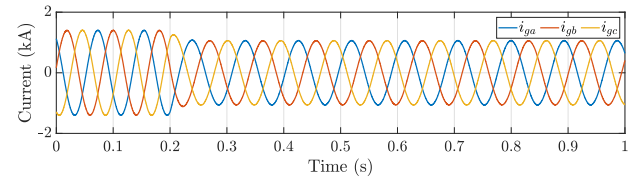
Fig. 8(d) shows the capacitors voltages of the rectifier phase a. The voltages of the upper arm submodules are balanced, as well as the voltages of the lower arm submodules. It is possible to verify the 10% voltage ripple stipulated in the capacitance design, since the voltages remain between 2.925 kV and 3.575 kV, with small transient variations. Fig. 8(e) shows the arm currents and the circulating current of the rectifier phase a. Except for the transient period after the wind speed variation, the second harmonic in the arm currents is suppressed and the circulating current i_{Kga} has only a DC component.



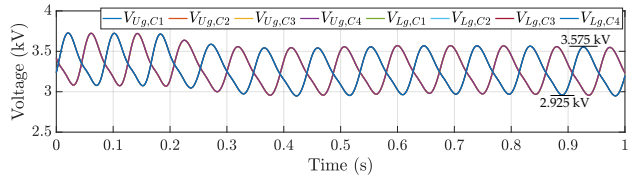
(a) Torques and angular speed of the turbine/generator shaft.



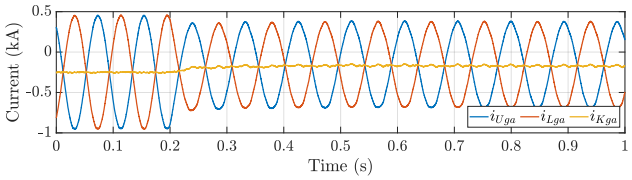
(b) Rectifier line voltage between phases a and b.



(c) Generator three-phase currents.



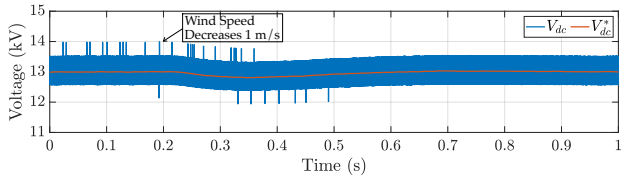
(d) Capacitor voltages of the rectifier submodules.



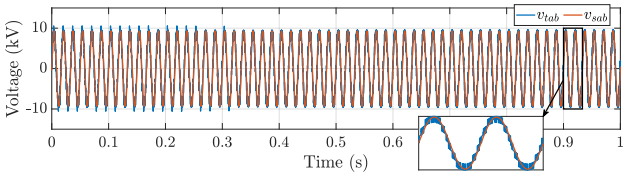
(e) Arm currents and circulating currents of the rectifier.

FIGURE 8. Waveforms of the rectifier MMC using LS-PWM strategy with sampling period of 1 µs and 10x subsampling.

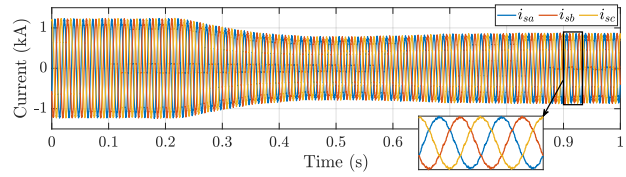
Fig. 9 shows the results of the inverter side, for the same test of Fig. 8, using LS-PWM with 10x subsampling ratio. Despite the higher frequency of the inverter, the same time range simulated is shown in Fig. 9. Fig. 9(a) shows the dc link voltage and its reference value 13 kV. The voltage ripple comes from the difference between the arm voltages, caused by the circulating currents control, however the average value is controlled and tracks its reference.



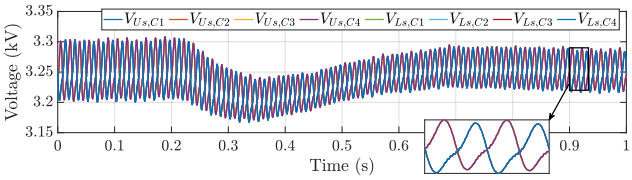
(a) DC link voltage with its reference value.



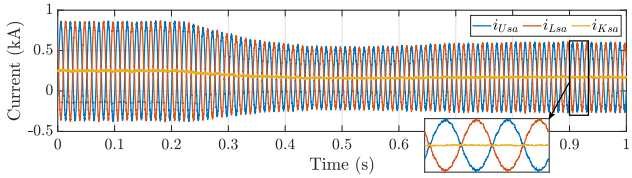
(b) Inverter and grid line voltages between phases a and b.



(c) Inverter three-phase currents.



(d) Capacitor voltages of the inverter submodules.



(e) Arm currents and circulating currents of the inverter.

FIGURE 9. Waveforms of the inverter MMC using LS-PWM strategy with sampling period of 1 µs and 10x subsampling.

Fig. 9(b) and Fig. 9(c) show the line voltages of the inverter and the grid and the three-phase currents, respectively. The terminal voltage v_{tab} has its levels more visible than the rectifier voltage, due to the smaller arm inductance of the inverter. The three-phase currents waveform is almost sinusoidal, even with the 10x subsampling ratio. The slow response of the DC voltage controller causes a smooth transient oscillation in the three-phase currents, in order to keep a stable operation.

Fig. 9(d) shows the capacitors voltages of the inverter phase a. It is possible to observe the voltages balanced in an

arm, however there is a small oscillation in the average value, inherent to the DC link voltage controller. The ripple of the submodules voltage is approximately 3%, much smaller than the 10% of the rectifier, since the same capacitance value was used at both converters. Fig. 9(e) shows the arm currents and the circulating current of inverter phase *a*. As well as at the rectifier, the circulating currents of the inverter has the second harmonic suppressed, remaining only the average value.

The waveforms of Fig. 8 and Fig. 9 show the dynamic stability of the proposed system when a wind speed variation is applied. Other operation conditions can be investigated in future studies, such as reactive power supplying, low-voltage ride-through operation and fault ride-through capability. In order to analyse the effects of the three modulation strategies and the subsampling ratio, the steady-state three-phase currents injected in the grid are presented next.

B. Steady-State Operation

The system of Fig. 1 was simulated in rated conditions, with wind speed of $12.3\ \mathrm{m/s}$ and using NLM, LS-PWM and PS-PWM strategies with a simulation step of 1 µs and subsampling ratios of 1x, 10x, 100x and 200x. The three-phase currents of the inverter side were the most affected variables, due to the higher frequency of the grid compared to the generator. Fig. 10(a), Fig. 10(b) e Fig. 10(c) show the three-phase currents of the inverter side, using NLM strategy with subsampling ratio of 10x, 100x and 200x, respectively. With a 10x subsampling ratio the currents are strongly affected by the 5th and 7th harmonics, which are characteristic of the NLM. Increasing the subsampling ratio, the 5th and 7th harmonics are reduced, but the currents become more distorted.

Fig. 11(a), Fig. 11(b) e Fig. 11(c) show the three-phase currents of the inverter side, using LS-PWM strategy with subsampling ratio of 10x, 100x and 200x, respectively. This strategy is least affected by the increase in the subsampling ratio. In addition, the currents synthesized by the LS-PWM have a lower harmonic content, presenting an almost sinusoidal waveform even for a 200x subsampling ratio. The harmonics caused by the LS-PWM are around the carrier frequency $1260\ \mathrm{Hz}$, while the switching frequency caused by the equalization algorithm are in $(200 \times 1\ \mu\mathrm{s})^{-1} = 5000\ \mathrm{Hz}$. Therefore, there is no harmonic overlap for 200x subsampling ratio.

Fig. 12(a), Fig. 12(b) e Fig. 12(c) show the three-phase currents of the inverter side, using PS-PWM strategy with subsampling ratio of 10x, 100x and 200x, respectively. The currents produced by the PS-PWM strategy present the lowest harmonic content with 10x subsampling ratio. However, this strategy is the most affected when the subsampling ratio increases. Since the harmonics of PS-PWM are around $4 \times 1260\ \mathrm{Hz} = 5040\ \mathrm{Hz}$, there is overlap between them and the switching harmonics for a 200x subsampling ratio.

Table 4 shows the THD of the terminal line voltages and three-phase currents of the rectifier and inverter, for the three modulation strategies and for subsampling ratios of 1x, 10x, 100x and 200x. The THD of the signals was calculated using a built-in function in the PSCAD/EMTDC simulation package. This function is designed to work optimally with the online frequency scanner-based FFT component, which processes data in three stages: (*i*) low-pass filtering for anti-aliasing, (*ii*) sampling and Fourier transform, and (*iii*) phase and magnitude error correction. All calculations were performed online and were based on a sampled data window with 128 samples/cycle of the base frequency. Furthermore, although the sampling rate of the equalization algorithm was changed, the time step of all simulations was kept equal to $1\ \mu\mathrm{s}$.

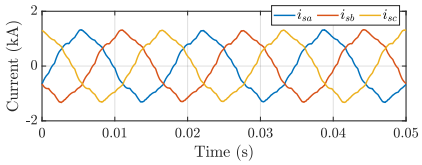
Although the collector network in Fig. 1 is isolated, as stated in [30], electric networks with a nominal voltage of $69\ \mathrm{kV}$ or lower have a recommended maximum total harmonic distortion (THD) of 5 %. The differences in THD between the 1x and 10x subsampling ratios are minimal. While the PS-PWM strategy shows the lowest THD at a 1x subsampling ratio, it exhibits the highest THD at a 200x subsampling ratio for the rectifier and inverter currents. The LS-PWM strategy, on the other hand, displays the least increase in THD for currents on both sides as the subsampling ratio rises. The NLM strategy introduces low-order harmonic distortions in the currents, which worsen with increasing subsampling ratios.

The last column of Table 4 presents the overall efficiency of the WEC system. This efficiency index was calculated as the ratio between the electrical power measured at the coupling point with the AC grid and the mechanical power measured at the turbine shaft. It is observed that the system's efficiency is minimally affected by the subsampling rate, showing a slight improvement when using LS-PWM. However, it is important to mention that the semiconductor switches in the PSCAD/EMTDC environment account only for conduction losses and do not include commutation losses. As a result, experimental models of this topology may yield different results compared to those observed in simulations.

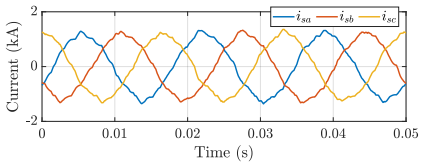
Since the same sampling period and carrier frequency were used for both converters, rectifier and inverter, the generator currents are less affected by the decreasing of the sampling frequency. Analyzing the THD of the generator's currents $i_{g,abc}$ in Table 4, it is possible to observe a significant impact only for 200x subsampling. In this sense, the waveform of the generator currents in steady-state are not shown in this paper, as the inverter currents in Fig. 10, Fig. 11 and Fig. 12.

VI. CONCLUSIONS

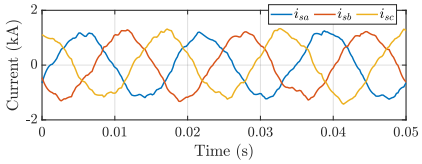
This paper proposed a wind energy conversion system for a $12\ \mathrm{MW}$ wind turbine, using a direct-drive generator and a back-to-back modular multilevel converter. It was discussed the control strategy used for the rectifier and the inverter, as



(a) Subsampling ratio 10x.

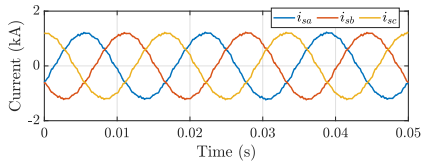


(b) Subsampling ratio 100x.

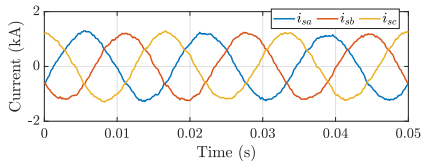


(c) Subsampling ratio 200x.

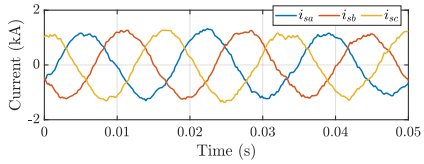
FIGURE 10. Steady-state three-phase currents of the inverter using NLM with sampling period of 1 μs.



(a) Subsampling ratio 10x.

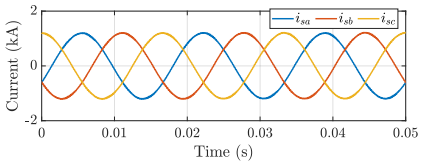


(b) Subsampling ratio 100x.

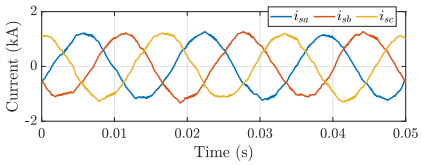


(c) Subsampling ratio 200x.

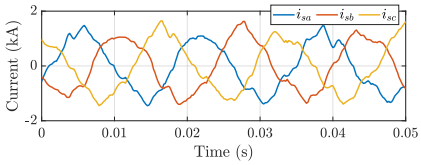
FIGURE 11. Steady-state three-phase currents of the inverter using LS-PWM with sampling period of 1 μs.



(a) Subsampling ratio 10x.



(b) Subsampling ratio 100x.



(c) Subsampling ratio 200x.

FIGURE 12. Steady-state three-phase currents of the inverter using PS-PWM with simulation step of 1 μs.

TABLE 4. THD of rectifier and inverter terminal voltages and line currents, and efficiency of the WEC unit, considering different modulation strategies and subsampling rates.

Modulation	Subsampling	THD (%)				η(%)
		v_{gab}	$i_{g,abc}$	v_{tab}	$i_{s,abc}$	
NLM	1x	2.0	0.9	10.4	6.8	87.7
	10x	2.3	0.9	10.1	6.6	87.7
	100x	7.7	0.8	10.2	5.5	88.9
	200x	6.6	1.1	9.1	8.7	89.4
LS-PWM	1x	8.5	0.4	12.3	2.6	87.7
	10x	8.4	0.4	12.0	2.7	88.0
	100x	8.9	0.6	9.9	4.6	89.1
	200x	7.2	1.1	11.0	6.7	90.4
PS-PWM	1x	15.8	0.2	19.6	1.3	87.7
	10x	15.9	0.2	19.6	1.4	88.3
	100x	12.4	0.8	14.9	6.4	88.6
	200x	8.1	1.7	16.7	18.8	89.7

well as a method to design the capacitances and inductances of the MMC arms. Simulations results were used to verify the dynamic and steady-state performance of the proposed system and to compare three modulation strategies: NLM, LS-PWM and PS-PWM.

It was possible to observe the effect of the equalization algorithm over the switching stress of the submodules. Using an equalization algorithm, the switching frequency is not proportional to the carrier frequencies, but related to the sampling frequency. Even for te NLM strategy there is a large number of commutations using the equalization algorithm. To mitigate this issue, a subsampling ratio was used to reduce the number of commutations, however, the quality of the voltages and currents synthesized by the converters has deteriorated.

The results allow to conclude that the NLM strategy does not reduce the switching stress if an equalization algorithm is used. In addition, although the PS-PWM strategy produces the lowest harmonic content without subsampling, it is most affected when the subsampling ratio increases. Furthermore, the LS-PWM strategy is less affected by the subsampling and does not increase the number of commutations. Finally, it is important to avoid overlap between the sampling frequency and the harmonic component produced by the modulation strategy.

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AUTHOR'S CONTRIBUTIONS

ALMEIDA, A.O.: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **PAULO, M.S.**: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation. **TEIXEIRA, D.P.**: Conceptualization,

Formal Analysis, Visualization. **VALLE, R.L.**: Conceptualization, Formal Analysis, Visualization. **ALMEIDA, P.M.**: Conceptualization, Formal Analysis, Funding Acquisition, Project Administration, Resources, Supervision. **BARBOSA, P.G.**: Conceptualization, Formal Analysis, Funding Acquisition, Investigation, Methodology, Project Administration, Resources, Supervision, Visualization, Writing – Original Draft, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

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