Eletrônica de Potência
Open Journal of Power Electronics

Received July 06, 2024; accepted November 21, 2024; Date of publication December 05, 2024.
The review of this paper was arranged by Associate Editor Allan F. Cupertino and Editor-in-Chief Heverton A. Pereira.

*Digital Object Identifier http://doi.org/10.18618/REP.e202454*

# Switch-Level Interleaved Converter: Circuit Operation, Output Ripple and Circulating Current

**Vítor H. M. Biajo[1], Gideon I. C. Lobato[1], Sidelmo M. Silva[1]**

[1]Universidade Federal de Minas Gerais, Department of Electrical Engineering, Belo Horizonte, MG, Brazil.

e-mail: vbiajo@ufmg.br; gideonlobato@ufmg.br; sidelmo@ufmg.br.

**ABSTRACT** This paper discusses an interleaved converter topology for DC-AC conversion in power electronics applications. The proposed topology leverages a switch-level interleaving technique to overcome the limitations of conventional interleaved inverters. Through comprehensive analysis and simulation studies, it is demonstrated that the interleaved inverter achieves higher power density and improved ripple frequency as compared to conventional counterparts. In this paper, different figures of merit are considered in order to assess the proposed converter scheme performance —such as current ripple parameters, circulating current and semiconductor losses. One of the main advantages of the proposed technology over conventional interleaving converters is the use of a single inductor, which enables its use not only in grid-tied applications but also in electric drives.

**KEYWORDS** DC-AC conversion, pulse-width modulation, single-phase inverters, interleaved converters.

## I. INTRODUCTION

Switched inverters have been widely employed in various industry sectors, electrifying systems and applications to meet productivity, economical and environmental targets. From light-weight (e.g. medical, robotics) to heavy-industry applications (e.g. energy, mining), power converters can be part of active-filters, electrical drives, and energy storage systems. For single-phase applications, the H-Bridge converter topology has been highly applied in grid-connected applications —solely or part of multistage converters [1]–[4]. For three-phase systems, the two-level inverter is the most common topology ever utilized, being extensively used in traction drives, industrial applications and grid-connected systems [5]–[7]. For medium power rated applications, multilevel converters and the Cascaded H-Bridge Modular Converter have been highly employed topologies, as they provide enhanced power quality and modular applicability, respectively [8], [9].

Further research has been conducted in order to improve key-metrics of inverter design, such as power density, efficiency and power quality [10]. These are essential parameters which enable the state-of-the-art electrified systems to become more compact, efficient and reliable. However, as the inverter rated power increases, the aforementioned inverter topologies present important drawbacks, such as large filter components, high harmonic distortion and slow dynamic response [11]. In this scenario, interleaved converters play a special role allowing the achievement of higher power densities with increased output power quality. By paralleling converters and phase-shifting their commands, these converters can not only diminish the filter size by increasing the ripple frequency, but also enhance the reliability of the system where they are installed, given their intrinsic fault-tolerance characteristic [12]. A conventional interleaved half-bridge is shown in Figure 1, where two half-bridges, with their respective output inductors, are connected in parallel to sum-up the output currents and therefore, achieve the objective of increasing the ripple frequency.

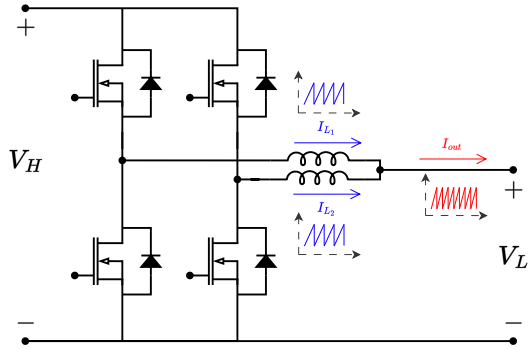


**FIGURE 1. Example of an interleaved half-bridge topology.**

The simple implementation of interleaved half-bridges turns the design of interleaved DC-DC converters to be slightly straight-forward, and basic principles of interleaving channels can be observed in these applications, sustained by the vast number of research present in the current literature. References [13]–[15] show the use of interleaved DC-DC converters to integrate different energy storage systems with challenging current and output ripple constraints. The work presented in [16] presents the design of a sixteen-phases synchronous buck converter for automotive applications. Reference [17] introduces the use of bi-directional DC-DC converters in a charging station for electric and hybrid

vehicles. Despite their benefits, interleaved converters can have the current imbalance among the phases as a major drawback. However, the use of coupled inductors has also been identified as one of the main researched solutions to address this problem as referenced in [18], [19], by the cost of increasing the design complexity and the voltage stress on the switches. Reference [20] proposes a control method to help mitigating this effect, by using FPGA to improve accuracy of switching pulses, but at a higher product cost. Among other proposals, the one presented in [21] details a solution that increases the converter power density and mitigates the current imbalance through a different modulation technique, implemented in a conventional DSP.

DC-AC converters can also inherit benefits from the interleaved half-bridge implementation, as different research papers have shown [11], [12], [22]–[27]. Reference [11] proposes the design of an interleaved three-phase inverter for grid-connected applications, achieving hardware volume reduction and higher dynamic capability. In addition, the use of interleaved inverters in grid-connected applications, especially for photovoltaic systems, can enhance the output power quality and improve ride-through capability for three-phase [12] and single-phase systems [22]. However, interleaved inverters can present circulating current due to asymmetries in the phase currents, contributing to increased stress on semiconductor switches and overall power losses [23]. Different works address this problem, by changing the control and modulation scheme [23]–[27]. Although different strategies have already been proposed to mitigate some important drawbacks, the solutions might come with important costs —such as increased complexity of control architecture, hardware and magnetics design.

Different from conventional interleaved converters, which rely on interleaving the modulation carriers, this paper discusses the Switch-Level Interleaved Converter (SLIC) —which was presented in [28] and operates by interleaving or intercalating the gate commands of its associated converter structure. In this paper, further details on circuit aspects, such as current ripple and circulating current analysis will be presented, as well as results of the modulation implemented under a digital signal processor (DSP) integrated into a hardware-in-the-loop (HIL) platform. Figure 2 illustrates the $M$-channel three-phase switch-level interleaved converter, where all interleaving channels of the same phase are paralleled connected, but sequentially commanded by a dedicated pulse-width modulation technique. This setup demonstrates that this technology serves not only to grid-connected applications, but also to electric drives as it does not require output inductors for each interleaving channel. As it can be applicable to different inverter topologies and applications, a single-phase current-controlled topology will be detailed in this work for the sake of simplicity. The hardware design and modulation technique will be detailed and explored to achieve a high performance in terms of ripple reduction, power density and dynamic capability. The proposed converter takes credit of the interleaved pulse-width modulation (IPWM) strategy, proposed in [21] for a DC-DC converter. Section II is focused on the concept of interleaving along with a detailed analysis of the IPWM. Section III discusses the system architecture, its implementation and filter inductance design considering particularities of the interleaved inverter. Section V presents the simulation results and compares different types of modulation for interleaved inverters.

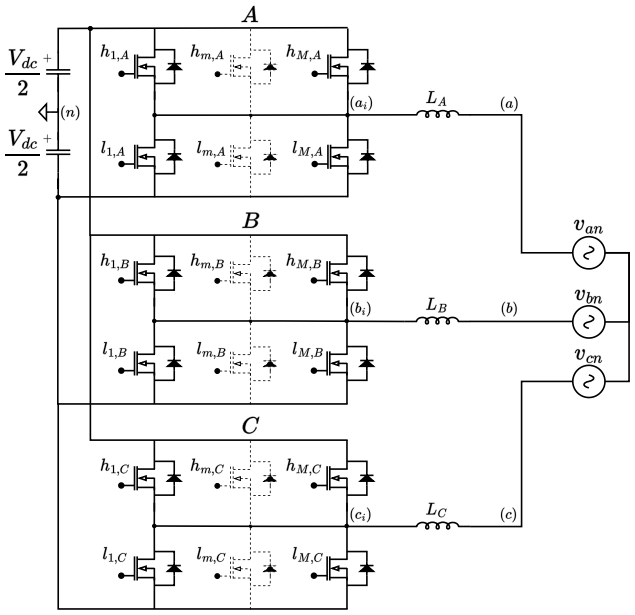


**FIGURE 2. M-channel three-phase switch-level interleaved converter.**

## II. CONVERTER TOPOLOGY AND MODULATION TECHNIQUE

### *A. Conventional Pulse-Width Modulation (CPWM)*

A single-phase interleaved inverter with a conventional pulse-width modulation (CPWM) is shown in Figure 3. The topology is composed of a converter with $m = [1, M]$ interleaving channels, where $M$ is a positive integer. The converter half-bridges are labeled as follows: $h_{m,A}$ and $l_{m,A}$ represent the $m^{th}$ high-side and low-side transistors for the phase A, respectively. Consequently, $h_{m,B}$ and $l_{m,B}$ represent the equivalent for the phase B. Furthermore, for each half-bridge output, an inductance with value $L_{m,A}$ or $L_{m,B}$ is being considered constituting a L-filter for the sake of simplicity, as opposed to a typical LCL filter, which would be the most appropriate choice for a current-controlled inverter application.

A traditional approach to control this inverter is through the phase-shifting pulse-width modulation (PS-PWM), so-called CPWM [29]. With this technique, each $m^{th}$ carrier is phase shifed by $2\pi/m$ *rad*. The modulated signals are generated based on the inverter number of phases, depending on whether unipolar or bipolar PWM is used [30]. As an example, for a dual-channel ($M = 2$) interleaved single-

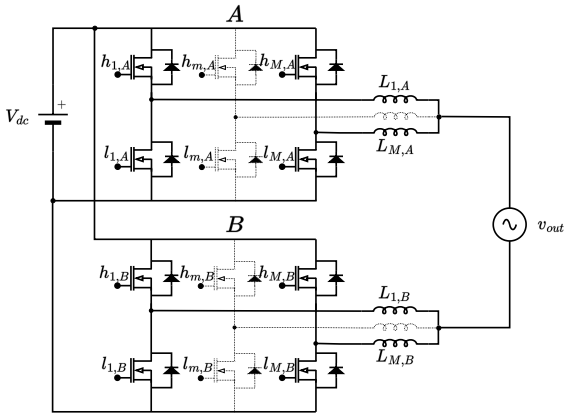


**FIGURE 3. Hardware topology of a M-channel single-phase interleaved inverter with conventional pulse-width modulation (CPWM).**

phase inverter, the channel carriers should be phase-shifted by $\pi$ *rad* between each other. Furthermore, a unipolar CPWM could be considered. This leads to a phase shift of $\pi$ *rad* between the modulated signals.

Figure 4 details the main waveforms for a dual-channel interleaved single-phase inverter with unipolar CPWM. It illustrates the PWM waveforms, such as the carriers and modulated signals for phase A and B. The waveforms shown in Figures 4-(b) to 4-(d) present the command signals for the switches, which can be generated by means of PWM comparison units in digital signal processors or other similar controllers. It is possible to note that channel commands are phase shifted, but still superpose each other. Figures 4-(f) to 4-(g) detail the inverter output voltage profiles. Finally, Figure 4-(h) details the addition of inductor currents, resulting in a higher frequency output ripple, given by $f_{ripple} = M \cdot f_{sw}$.

### *B. Interleaved Pulse-Width Modulation (IPWM)*

A generic single-phase interleaved inverter with IPWM is shown in Figure 5. As compared with the conventional topology, the SLIC is composed of half-bridges, labeled in a similar fashion. The main difference stands in the direct connection among the $M$ channels, and the consequent single output inductors, labeled as $L_A$ and $L_B$, which could be added together into a unique $L_{AB}$ inductor.

Figure 6 presents the characteristic waveforms for the IPWM. The first set of waveforms detail the carriers and modulated signals. The modulated signals remain the same as for CPWM, as they represent the expected output waveforms. However, different from the CPWM, the carrier frequency is given by $f_{carrier} = M \times f_{sw}$, and each switch is to operate once every *M* carrier cycles. This fact is better illustrated in Figures 6-(b) to 6-(e), which detail the gate commands for the transistors, along with a switch counter $k_m(t)$ for enabling and disabling the commands for the $m^{th}$ channel. When $k_m(t) = 1$, the first channel is activated. Consequently, when $k_m(t) = 2$, the second channel is

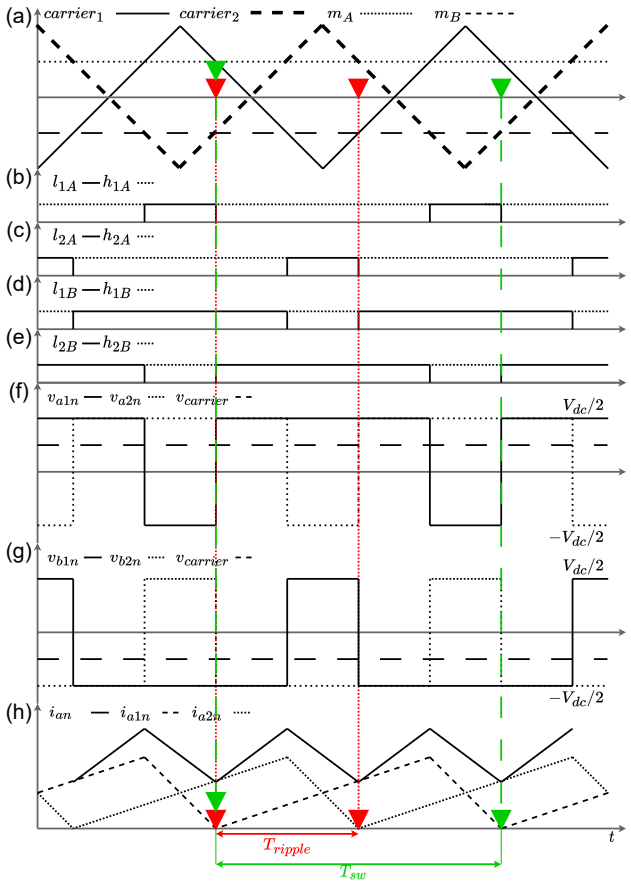


**FIGURE 4. Main waveforms for a dual-channel interleaved inverter with CPWM.**

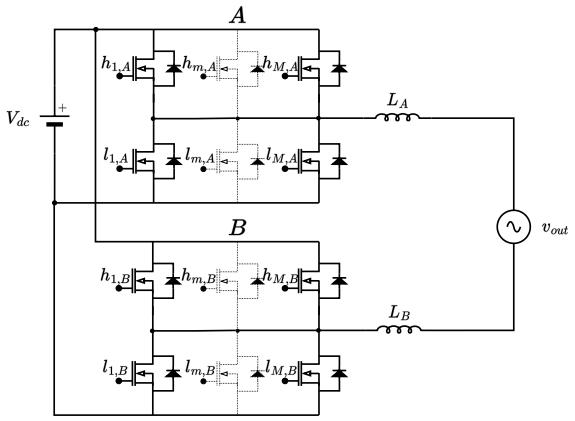


**FIGURE 5. Hardware topology of a M-channel single-phase interleaved inverter with interleaved pulse-width modulation (IPWM).**

activated, and the remaining one is deactivated. This set of waveforms illustrate the IPWM operation, where the pulses are interleaved with each other, producing a high-frequency inverter output voltage waveform, as illustrated by 6-(g) and 6-(h). Finally, different from the CPWM, the resulting output ripple is not a consequence of output inductor currents addition, but of the *M* inverters output voltage superposition.

The output current and its ripple frequency is illustrated in Figure 6-(i), contributing to (1).

$$f_{ripple} = 2 \cdot f_{carrier} = 2 \cdot M \cdot f_{sw} \tag{1}$$

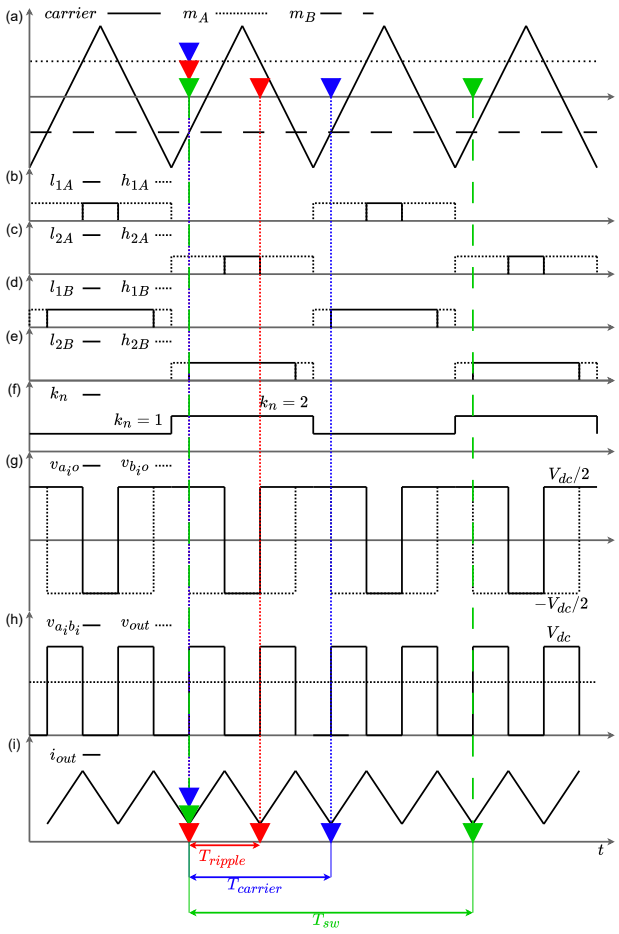


**FIGURE 6. Main waveforms for a dual-channel inverter with IPWM.**

### C. Ripple Reduction

As mentioned, ripple reduction can be obtained with the interleaving commands and voltage superposition at the inverter bridge output, as especially shown in Figure 6-(g) to 6-(h). One may note that output waveforms have been illustrated by considering $f_{carrier} \gg f_g$. Furthermore, for a simple approach of the dual-channel single-phase SLIC as shown in Figure 7, the voltage drop across the output inductor $L_{AB}$ is given by (2).

$$v_{L_{AB}} = \frac{L_{AB} \cdot \Delta i_L}{T_{on}} \tag{2}$$

In (2), $T_{on}$ represents the equivalent on-time of the inverter output, or when the line voltage is momentarily equal to $\pm V_{dc}$, as shown in Figure 6, and $i_L$ represents the phase current flowing through the inductor. Furthermore, by knowing $T_{on}$ can be expressed as function of the duty-cycle $d(t)$

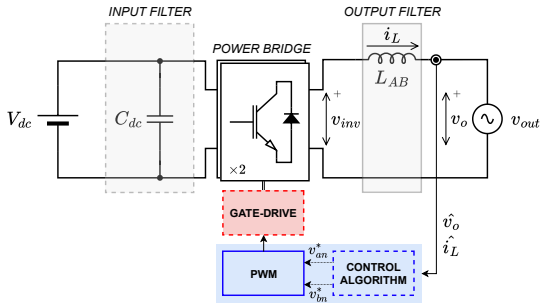


**FIGURE 7. System architecture and simplified circuit diagram for the dual-channel single phase inverter.**

and $f_{ripple}$ and applying (1), (2) is rearranged and the ripple current excursion is given by (3).

$$\Delta i_L = \frac{d(t) \cdot (V_{dc} - v_o(t))}{2 \cdot L_{AB} \cdot f_{carrier}} \tag{3}$$

As detailed in [31], equation 3 can be further developed into (4) considering $v_o(t) = m_a \cdot V_{dc} \cdot sin(\omega t)$ and $d(t) = m_a \cdot sin(\omega t)$, where $m_a$ represents the modulation index.

$$\Delta i_L = \frac{m_a \cdot sin(\omega t) \cdot V_{dc} \cdot (1 - m_a \cdot sin(\omega t))}{2 \cdot L_{AB} \cdot f_{carrier}} \tag{4}$$

In order to find the maximum current ripple, (4) can be differentiated in terms of $\omega t$ and equation 5 can be solved.

$$\frac{\mathrm{d}}{\mathrm{d}\omega t} K \cdot sin(\omega t)(1 - m_a \cdot sin(\omega t)) = 0 \tag{5}$$

where $K = (m_a \cdot V_{dc})/(2 \cdot L_{AB} \cdot f_{carrier})$.
Solving (5) for $\omega t$, equation roots are expressed by (6).

$$\omega t = \begin{cases} i) \ (2n+1)\frac{\pi}{2} \ \forall \ n \in \mathbb{Z} \\ ii) \ sin^{-1}\frac{1}{2m_a}, \ m_a \neq 0 \end{cases} \tag{6}$$

The first solution $(i)$ gives the maximum ripple for a particular condition where $0 < m_a < 0.5$. Considering an application where $m_a > 0.5$, the second solution $(ii)$ is chosen for the maximum ripple which is obtained substituting (6) into (4), resulting in equation 7.

$$\Delta i_L = \frac{V_{dc}}{8 \cdot L_{AB} \cdot f_{carrier}} \tag{7}$$

Equation 7 reveals that the higher the carrier frequency, the lower the inductor current ripple amplitude. This adjustment to the carrier frequency can be obtained by setting up the controller parameters, depending on the capabilities of the hardware circuit. Nevertheless, as defined in (1), the carrier frequency is also dependent on the switching frequency and the number of interleaving channels, imposing an important trade-off to consider for the converter design. Therefore, assuming that the carrier frequency would be adjusted by a controller to keep the semiconductors switching frequency constant, increasing the number of interleaving channels

would not only raise the ripple frequency but also reduce the current ripple amplitude, allowing for a smaller inductor, as compared to a conventional inverter topology.

### D. Circulating Current

Circulating current represents a current component which flows between parallel inverters, which can operate with interleaved commands. Two groups of circulating currents can be identified: 1) low-frequency circulating current, which is described in [32], appearing as a beat wave which envelopes the fundamental component; and 2) high-frequency circulating current, which occurs due to asymmetries existing in the circuit with components represented at a multiple of switching frequencies [33]. These circulating currents can result in higher losses in the semiconductors and increased electromagnetic interference, due to higher common-mode emissions.

Figure 8 shows a representation of zero-vector switching state and its resulting circuit scheme, which allows the flow of circulating current between the inverters in parallel. Considering this current path, and as defined in [33], the circulating current for a conventional interleaved inverter can be calculated as described in (8), where $\Phi$ represents the phase in a multiphase system.

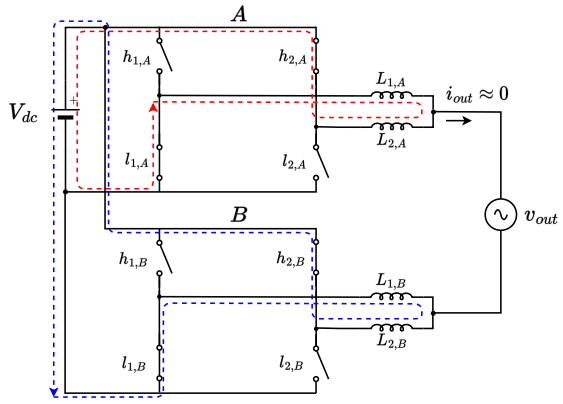


**FIGURE 8. Zero-vector switching state for the dual-channel interleaved single-phase inverter with CPWM.**

$$i_{\Phi_c} = \frac{i_{1,\Phi} - i_{2,\Phi}}{2} \tag{8}$$

As opposed to the conventional interleaved converter, in a normal operating condition, no circulating current would be expected in the operation of the SLIC, as illustrated in Figure 9. However, this is not a practical and realistic consideration, given that non-idealities of the semiconductor switches and the power electronics mechanical assembly can lead to a current imbalance. In the end, this current imbalance has similar effects as compared to the circulating currents, especially during reverse conduction of diodes during zero states when free-wheeling occurs.

With this established, it is possible to define an effective equation to estimate this circulating current effect generated

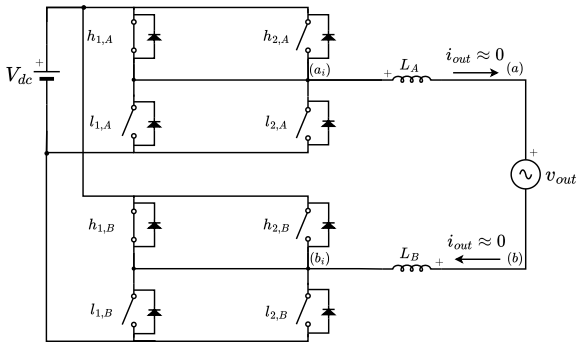


**FIGURE 9. Zero-vector switching state for the dual-channel switch-level interleaved single-phase inverter with IPWM.**

by current imbalance of SLIC, as shown in (9). The terms of this equation are detailed in Figure 10, which is a rearranged representation of the circuit of the same proposed converter, for phase A. Note this equation depends on a established condition, which arises due to the impracticality of representing the switch-level interleaving scheme with a linear equation.

$$i_{\Phi_c} = \frac{i_{1,\Phi} - i_{2,\Phi}}{2} \leftrightarrow [2 \times i_{\Phi_c} \neq i_{\Phi}] \tag{9}$$

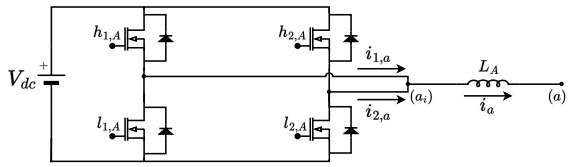


**FIGURE 10. Circuit diagram for circulating current calculation of SLIC with IPWM.**

Finally, in order to have a proper comparison of the impact of circulating current in both conventional and the proposed converter, circulating current amplitude value can be evaluated against line current contribution as a figure of merit. Therefore, a circulating current factor is defined in (10), where $I_c$ represents the peak value for the circulating current and $I_{out}$ the peak of the output current.

$$K_{cc} = \frac{I_c}{I_{out}} \times 100 \tag{10}$$

## III. SYSTEM DESIGN

### A. Architecture

Having presented the power bridge topology and the IPWM concept for the proposed converter, this section focuses on the converter system architecture, as shown in Figure 7.

As a general description, the first sub-system is the input filter, directly connected to the DC link, and which needs to be designed in order to eliminate current harmonics flowing to the DC voltage source. The second block is the power-bridge, which has already been detailed in Figure 5. This

sub-system is mainly composed by the semiconductors, in which could be encapsulated in a single case, providing better thermal coupling and avoiding current imbalance among the interleaving channels. Next there is output filter, constituted by a single inductor, as a current-controlled inverter is being considered. The controller unit is also shown as the composition of two different parts: the control algorithm and the modulation processing function. Lastly, the gate-driver system is shown, connecting the controller to the power-bridge, for commanding and monitoring functions.

Two sets of sub-systems can be identified: 1) the ones with dashed lines, which will not be detailed in this work; 2) the remaining ones with solid lines, which will be further described in this section. This will contribute to present a practical implementation to be used in a simulation environment as an initial proof-of-concept for a future hardware setup.

### B. Filter Design

As a current-controlled inverter is in the scope of the present work, a L filter can be considered. The inductance calculation can be derived directly from (7) by isolating the inductance term, leading to the equation below.

$$L_{AB} = \frac{V_{dc}}{8 \cdot \Delta i_L \cdot f_{sw} \cdot M} \tag{11}$$

The maximum current ripple $\Delta i_L$ can be set as 15% of the nominal current [34]. By having determined the current ripple, the switching frequency $f_{sw}$, the DC voltage $V_{dc}$ and the number of interleaving channels $M$, the inductance can be determined.

### C. Modulation Scheme

The implementation of the IPWM demands a different approach as compared to the current available implementation of existing conventional PWM algorithms. Apart from the control strategy, a software block diagram is shown in Figure 11 and by considering only phase A modulation, it details the main functions to be performed when implementing this new modulation technique.

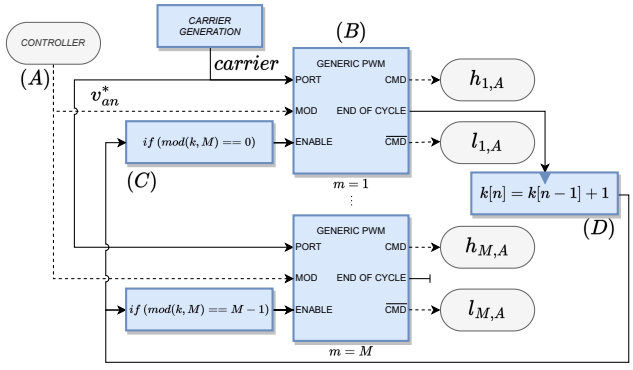


**FIGURE 11. Block diagram of the IPWM logic.**

**TABLE 1. Simulation parameters**

| Parameter | Variable | CPWM | IPWM |
|---|---|---|---|
| Apparent Power | $S_n$ | $12\ kVA$ | $12\ kVA$ |
| DC Voltage | $V_{dc}$ | $600\ V$ | $600\ V$ |
| Filter Inductor | $L_{AB}$ | $221\ \mu H$ | $221\ \mu H$ |
| Number of Channels | $M$ | 2 | 2 |
| Carrier Frequency | $f_{carrier}$ | $20\ kHz$ | $40\ kHz$ |
| Switching Frequency | $f_{sw}$ | $20\ kHz$ | $20\ kHz$ |
| Output Frequency | $f_g$ | $60\ Hz$ | $60\ Hz$ |
| Output Voltage | $V_o$ | $220\ V_{rms}$ | $220\ V_{rms}$ |

Firstly, the modulation signals are indicated by (A), where they can be the output signals of the control algorithm, or simply an open-loop input. The modulation signals feed into $M$ conventional PWM blocks ($2 \times M$, for dual-phase modulation), which are indicated as (B). Differently from legacy developments, these blocks must be configured using the carrier frequency, rather than the semiconductors switching frequency. The carriers should not be phase shifted among themselves, as shown in Figure 6. Additionally, these PWM blocks are tripped every time the logic detailed by (C) results in false, playing the role of the channel counter ($k_m$) in Figure 6. With this tripping system, the conventional PWM outputs will command the switches off for that period of time the $m^{th}$ channel should be disabled. The reference PWM block outputs an incremented counter at the end of every PWM cycle, at the carrier frequency. This feeds the IPWM counter logic, which is indicated by (D).

This modulation technique implementation results in interleaved commands for the semiconductors, behaving as shown in Section II.

## IV. SIMULATION RESULTS

A MATLAB Simulink model was developed for analyzing the preliminary results for both converters: 1) the conventional interleaved converter, as shown in Figure 3; and 2) the single-phase SLIC, detailed in Figure 5. Both converters work as step-down single-phase inverters for a current-controlled application. The simulation parameters are shown in Table 1. In this section, the terms CPWM and IPWM will be used not only for referencing to the modulation technique, but also to reference to the conventional interleaved converter and SLIC topologies.

### A. Output Current

Figure 12 shows the output current profiles for the CPWM and the IPWM. Both profiles have approximately the same phase and root mean square values of $54.4\ A$ and $53.9\ A$, respectively. Additionally, peak current values differ between the two modulation schemes, where $92.9\ A$ for the CPWM and $80.2\ A$ is obtained for the proposed modulation.

Apart from the fundamental component of the output current profiles, main harmonics are due to the ripple generated

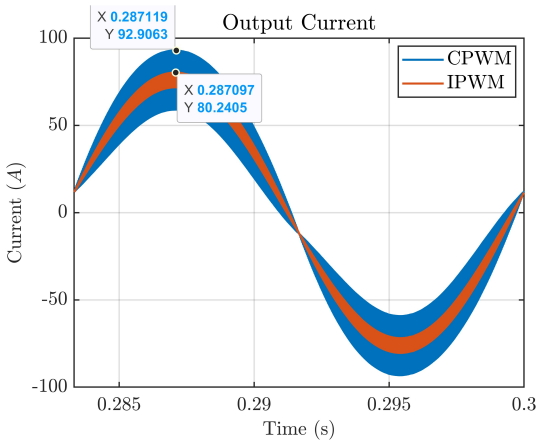


**FIGURE 12. Output current profiles for CPWM and IPWM.**

by the inverter switching behavior. The frequency spectrum is shown in Figure 13 for the output current for the both converters. Current magnitude values for the fundamental components remained similar, around $76.1\,A$ for both. However, for the next largest high-frequency harmonics, it is noticed that the CPWM presents a component of $40\,kHz$ with $6.7\,A$, whereas the IPWM has it at $80\,kHz$, with $1.6\,A$. Additionally, the total harmonic distortion for both current profiles resulted in $15.2\,\%$ and $3.8\,\%$ for CPWM and IPWM respectively.

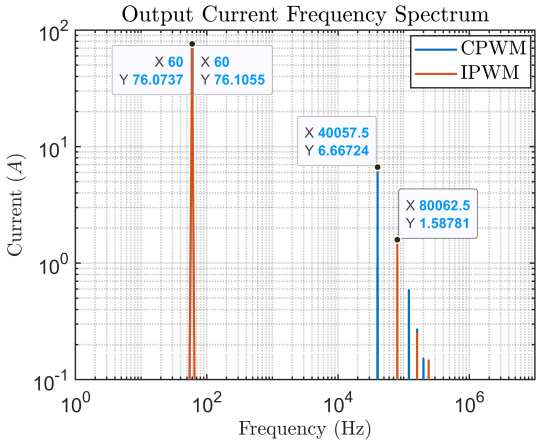


**FIGURE 13. Frequency spectrum of output current for CPWM and IPWM.**

In terms of actual ripple seen on the current-controlled side, Figure 14 highlights remaining current components apart from the fundamental one, as seen in Figure 12. Resulted ripple amplitudes are around $31.6\,A$ and $8.3\,A$ for both CPWM and IPWM, respectively. Note that these waveforms still include the low-frequency circulating currents.

Additionally, Figure 15 and 16 detail the ripple amplitude surfaces calculated using the methodology defined in [35] for CPWM, and Equation 4 for IPWM. The proposed converter presents lower ripple amplitudes throughout the entire surface maps. Figure 15 shows how the ripple amplitude varies with the number of channels, fixing the modulation index.

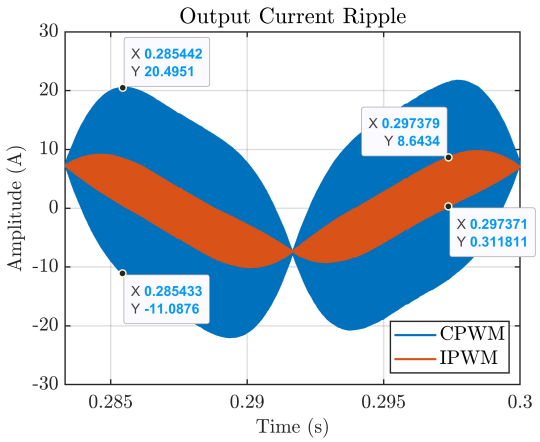


**FIGURE 14. Ripple profile for the output current for CPWM and IPWM.**

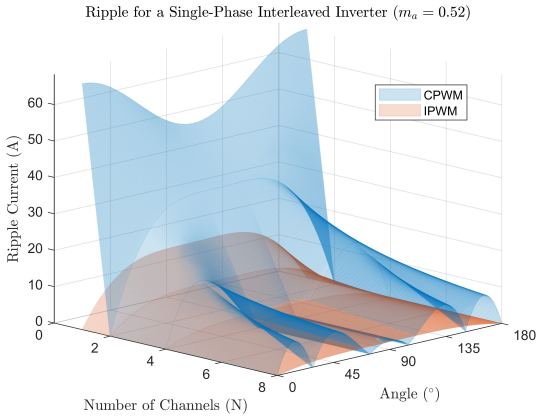


**FIGURE 15. Output current ripple for a single-phase interleaved inverter ($m_a = 0.52$), obtained from analytical calculation.**

Figure 16 details the ripple amplitudes as a function of the modulation index and sine wave angles, given a fixed number of interleaving channels. In particular, it is possible to observe that the surface maps have a similar aspect, apart from their amplitude values.

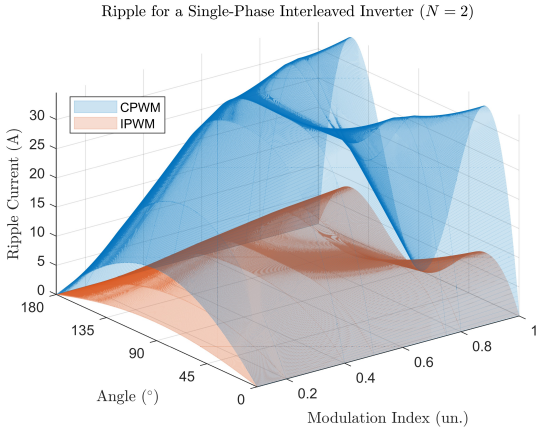


**FIGURE 16. Output current ripple for a single-phase interleaved inverter ($N = 2$), obtained from analytical calculation.**

In terms of analytically calculated current ripple, for CPWM, the output current ripple amplitude results in a value around $30\,A$ for a case where $N = 2$ and $m_a = 0.52$, which is the operation point of the simulated system. Whereas for IPWM, the resulting values are found between $5$ and $10\,A$. Both findings align with the simulated ripple results which are also detailed in this work.

### B. Inductor Current

Inductor current profiles can be seen in Figure 17. Both converters present significantly different results, as the CPWM and IPWM have a maximum amplitude current of around $62.9\,A$ and $80.2\,A$, respectively. Both current profiles were processed by the *Fast Fourier Transform* (FFT), leading to the results shown in Figure 18. Different from the ouput current profiles, here we can see that for the CPWM the inductor ripple differs from the output current ripple. In this case, the highest ripple harmonic is seen at $20.0\,kHz$ with $19.1\,A$ of current amplitude. Now for the IPWM, the values remain the same as for the output current already shown previously. This is due to the interleaving done at the switch level, not as a superposition of inductor currents.

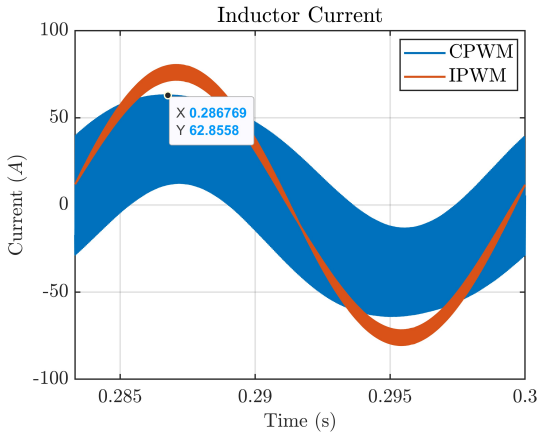


**FIGURE 17. Inductor current profiles for CPWM and IPWM.**

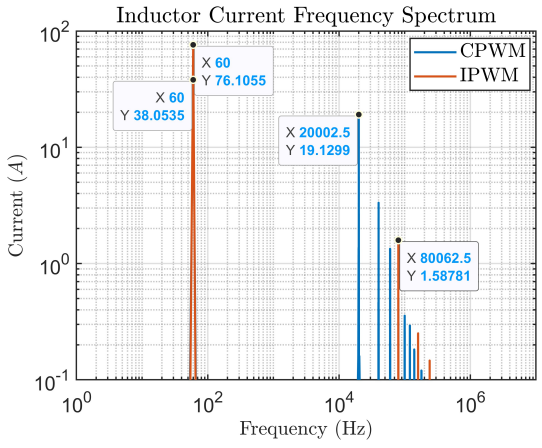


**FIGURE 18. Frequency spectrum of inductor current for CPWM and IPWM.**

Furthermore, the actual ripple amplitudes can be seen in Figure 19. The total inductor ripple amplitude results in $67.9\,A$ and $8.3\,A$ for CPWM and IPWM, respectively. The proposed modulation resulted in a ripple 8 times lower than the conventional one.

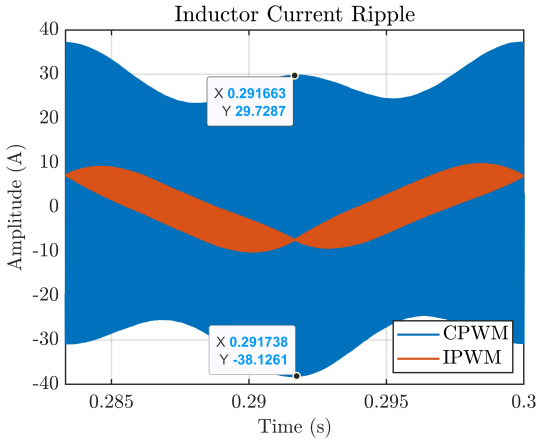


**FIGURE 19. Inductor current ripple for CPWM and IPWM.**

Finally, by evaluating (12), the maximum stored energy in the inductors can be estimated, which is a key factor for an inductor size, as defined in [30]. Considering the whole set of inductors for each topology, the resulting values are $1.12\,J$ for CPWM, and $0.74\,J$ in case of IPWM. This leads to a 33% of volume saving with the SLIC.

$$W_L = L \int i_L \cdot \mathrm{d}i_L \tag{12}$$

### C. Circulating Current

Figure 20 details both CPWM and IPWM circulating current profiles for the low-frequency region. These current profiles were calculated based on (8). It is possible to observe that the circulating current reaches a maximum of $34.65\,A$ of amplitude for the CPWM, having a low-frequency beating wave of 120 Hz, which is the double of the fundamental frequency. Given a peak output current amplitude of $92.42\,A$, the circulating current factor, as defined in (10), results in $37.5\%$.

For IPWM, the maximum values of output and circulating current result in $80.4\,A$ and $13.34$, respectively. These results leads to circulating current factor of $16.6\%$. Also note that the circulating current profile presents an enveloping wave at 120 Hz, double the fundamental frequency,

Figure 21 details the circulating current profiles around the maximum points of IPWM, zooming in to detail their high-frequency components. Both waveforms contain a high-frequency component at $20\,kHz$, which is the effective switching frequency of both converters. Note that the CPWM presents a continuous trapezoidal current profile, whereas the IPWM presents a more discontinuous circulating current profile. These aspects also lead to a different harmonic distribution throughout their frequency spectra, as shown in

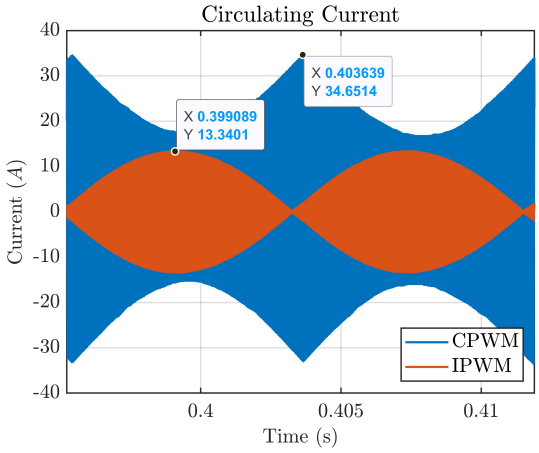


**FIGURE 20. Low-frequency circulating current comparison for CPWM and IPWM.**

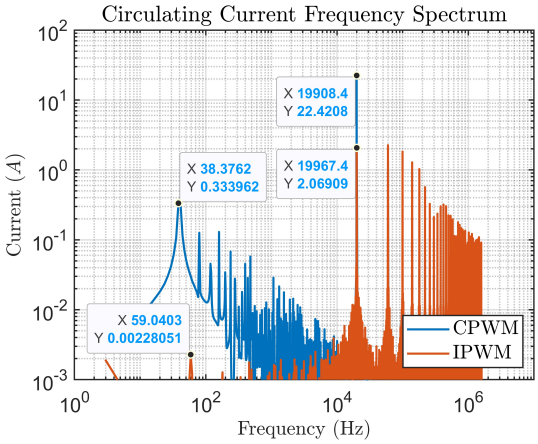


**FIGURE 22. Frequency spectrum of circulating current for CPWM and IPWM.**

Figure 22, which indicates that the CPWM presents a higher pollution at lower frequencies, whereas the IPWM has a dense harmonic content at higher frequencies.

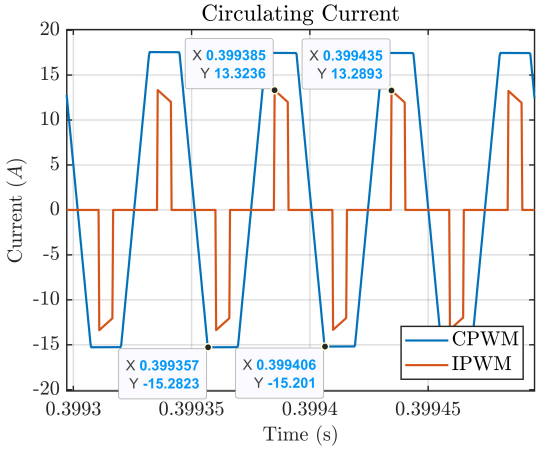


**FIGURE 21. High-frequency circulating current comparison for CPWM and IPWM.**

Furthermore, with the formulation defined in (9) and the switching waveforms presented in Figure 23 and 24, it is possible to conclude that the circulating current mainly occurs due to unequal current sharing during MOSFET and body diode reverse conduction, in case of IPWM.

### *D. Power Bridge*

The following results present the overall current conduction waveforms for the upper and lower switches of both converters. In this section, a 1200V-100A Silicon Carbide MOSFET power module was considered for switching and conduction losses calculation.

Figure 23 shows the respective profiles for the CPWM. The results show an expected performance of the conventional converter, as detailed in Figure 4. These waveforms were used in the transistors losses calculation, considering parameters detailed in Table 1. The switching losses resulted in $152.8\,W$ and the conduction losses in $42.4\,W$ for the transistors. Reverse recovery and conduction losses were estimated to be around $11.2\,W$ and $131.9\,W$ for all the diodes, respectively. The total losses resulted in $338.3\,W$, with an efficiency of $97.2\%$.

Similarly, the transistor current profiles for the IPWM are also shown in Figure 24. The preliminary results show a higher number of switching events for the upper switches as compared to the lower ones, resulted from the usage of a triangle carrier with the IPWM technique. This fact has not been noticed in [21], due to an initial implementation considering a sawtooth carrier. Furthermore, as the pulses do not superpose each other, the IPWM normally operates at hard-switching if controlled snubber circuits are not used. These observations are crucial for understanding the higher switching losses for the IPWM, as confirmed by the calculation. Switching and conduction losses resulted in $250.6\,W$ and $60.1\,W$ for the transistors, respectively. All diode losses included reverse recovery and conduction losses, being about $40.6\,W$ and $103.6\,W$. IPWM power bridge losses resulted in $454.9\,W$, leading to a $96.2\%$ efficient converter.

### *E. Results Comparison*

The presented results are synthesized in the Table 2. The output current ripple amplitude and frequency indicated to benefit SLIC over the conventional interleaved converter, given the credit taken from utilizing a unipolar IPWM with also increasing the ripple frequency by a factor of $M$. IPWM requires around $33\%$ lower volume for the inductors. The IPWM presents lower amplitude circulating currents, especially in the low-frequency range. For the high-frequency range, it shows to increase common-mode emissions. Important to note these results were obtained in a case of an almost ideal circuit condition, which needs to be validated via prototype testing. As expected, overall semiconductor losses showed to be higher for the IPWM than for the CPWM, leading to lower efficiency by $1\%$.

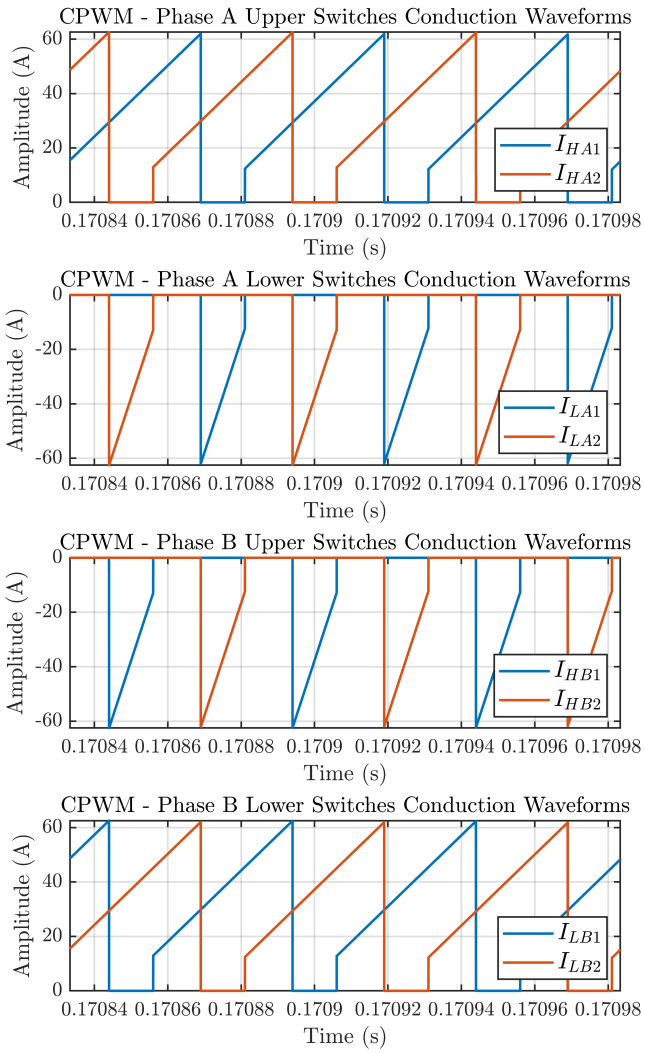


**FIGURE 23. Switches conduction profiles for the CPWM.**

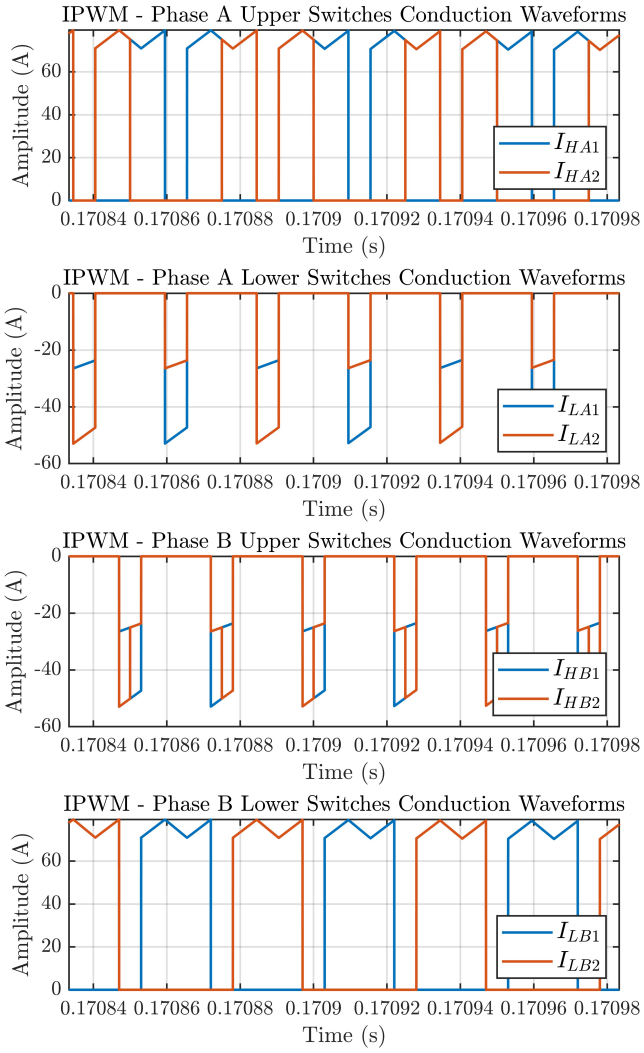


**FIGURE 24. Switches conduction profiles for the IPWM.**

**TABLE 2. Results Overview for CPWM and IPWM**

| Parameter | Unit | CPWM | IPWM |
|---|---|---|---|
| Output Current | $Arms$ | 54.4 | 53.9 |
| Output Current THD | % | 15.2 | 3.8 |
| Output Peak Current | $A$ | 92.9 | 80.2 |
| Output Current Ripple | $A$ | 31.6 | 8.3 |
| Output Current Ripple Frequency | $kHz$ | 40.0 | 80.0 |
| Inductor Peak Current | $A$ | 62.9 | 80.2 |
| Inductor Current Ripple | $A$ | 67.9 | 8.3 |
| Inductor Current Ripple Frequency | $kHz$ | 20.0 | 80.0 |
| Circulating Current Factor | % | 37.5 | 16.6 |
| Transistor Losses | $W$ | 195.2 | 310.7 |
| Diode Losses | $W$ | 143.1 | 144.2 |
| Total Losses | $W$ | 338.3 | 454.9 |
| Efficiency | % | 97.2 | 96.2 |
| Inductor Volume | p.u | 1.00 | 0.67 |

## V. HARDWARE-IN-THE-LOOP RESULTS

A HIL test bench was set up to validate the modulation and controller implementation of the SLIC. A HIL604 from Typhoon HIL was used for running the power electronics model. A Texas Instrument TMS320F28335 was used for the modulation commands and control implementation, as a DSP, in which the logic presented in Figure 11 was implemented.

The topologies described in Figure 3 and 5 were considered. The HIL test bench parameters are defined in Table 3. It is important to note that adjustments were made to the filter inductance, carrier frequency and switching frequency compared to those listed in Table 1, as target output current and ripple were kept the same. These adjustments were needed due to processing capability limits and numerical errors that occured during HIL simulations at high switching frequencies.

Figure 25 highlights the gate commands for the transistors, obtained as output signals of the DSP for the IPWM. Following the nomenclature detailed in subsection B, the

**TABLE 3. HIL Test Bench Parameters**

| Parameter | Variable | CPWM | IPWM |
|---|---|---|---|
| Apparent power | $S_n$ | $12\ kVA$ | $12\ kVA$ |
| DC voltage | $V_{dc}$ | $600\ V$ | $600\ V$ |
| Filter inductor | $L$ | $442\ \mu H$ | $442\ \mu H$ |
| Inductor series resistance | $r_L$ | $6.15m\Omega$ | $6.15m\Omega$ |
| Number of channels | $M$ | 2 | 2 |
| Carrier frequency | $f_{carrier}$ | $5\ kHz$ | $10\ kHz$ |
| Switching frequency | $f_{sw}$ | $5\ kHz$ | $5\ kHz$ |
| Output frequency | $f_g$ | $60\ Hz$ | $60\ Hz$ |
| Output voltage | $V_o$ | $220\ V_{rms}$ | $220\ V_{rms}$ |

transistor commands are defined as follows: $h_{1,A}$ as *digital input 32*, $h_{2,A}$ as *digital input 31*, $l_{1,A}$ as *digital input 26*, $l_{2,A}$ as *digital input 25*, $h_{1,B}$ as *digital input 30*, $h_{2,B}$ as *digital input 29*, $l_{1,B}$ as *digital input 24*, $l_{2,B}$ as *digital input 23*. This set of waveforms align with the theoretical ones detailed in Figure 6, indicating the effectiveness of the proposed modulation scheme implementation in a real controller.

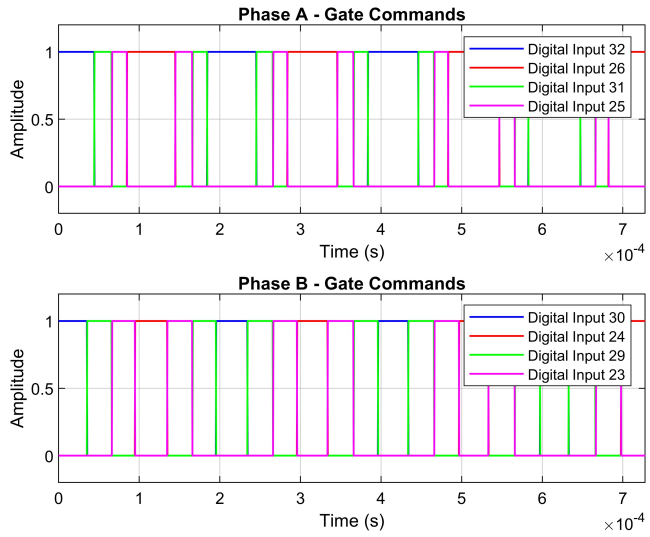


**FIGURE 25. IPWM gate commands, HIL simulation.**

With the proper implementation of gate commands, the output current measurements were detailed for a conceptual validation. At first, the results shown in Figure 26 demonstrate the similarity of the HIL simulation as compared to the offline simulation with results presented in Section IV, showing peak current values within $\pm 3\%$ of margin to the offline simulation baseline. A peak current value of $94.8\ A$ was obtained for CPWM, whereas IPWM resulted in a value of $81.9\ A$.

For extracting the ripple components, the output current profiles can be subject to a low-pass filter, resulting in the curves illustrated in Figure 27. A ripple amplitude of $28.1\ A$ was obtained for CPWM, and $7.4\ A$ for IPWM, revealing

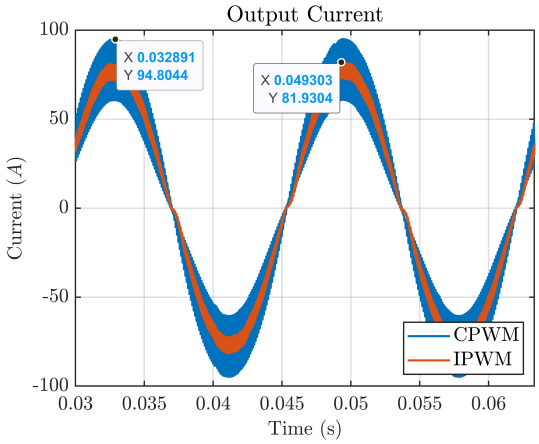


**FIGURE 26. Output current profiles for CPWM and IPWM, HIL simulation.**

around four times of ripple reduction for the proposed topology.

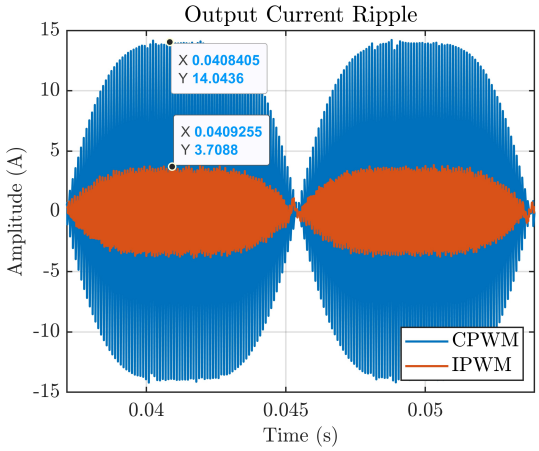


**FIGURE 27. Output current ripple profiles for CPWM and IPWM, HIL simulation.**

Harmonic content of output current profiles can be seen in Figure 28. Differently from the offline simulation results, IPWM shows a high harmonic pollution in the low-frequency region. Despite that, the total harmonic distortion of the current profiles resulted in $15.03\%$ and $5.01\%$ for both CPWM and IPWM, respectively.

## VI. CONCLUSION

This paper discussed the interleaved converter topology for DC-AC conversion, which demonstrated superior performance for ripple filtering and system dynamics, but worse overall efficiency as compared to the conventional inverter topologies. The proposed topology was tested in a simulation environment, which showed that it can effectively reduce the current ripple, improve the power factor, and increase the power output for a significantly smaller output filter, thus lower volume, weight and complexity, as it requires one single output inductor. Furthermore, an initial investigation was done to assess circulating current impacts in both converter

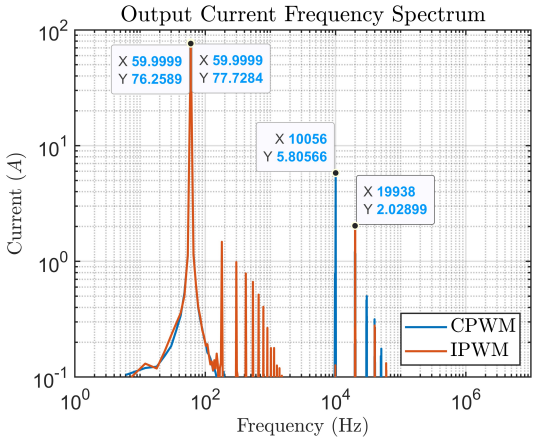


**FIGURE 28. Frequency spectrum of output current for CPWM and IPWM, HIL simulation.**

topologies. This research contributes to the development of high-performance and reliable power electronics systems for various applications, such as renewable energy systems, electric vehicles, and aerospace.

Further research could explore the possibility of integrating the proposed topology with converter control techniques to enhance its performance, and possibly improve the modulation technique for a better energy efficiency.

## ACKNOWLEDGMENT

This work was carried out with the support of the Coordination for the Improvement of Higher Education Personnel - Brazil (CAPES) through the Academic Excellence Program (PROEX).

## AUTHOR'S CONTRIBUTIONS

**BIAJO, V. H. M.**: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **LOBATO, G. I. C.**: Conceptualization, Investigation, Methodology, Software, Validation. **SILVA, S. M.**: Conceptualization, Funding Acquisition, Investigation, Methodology, Resources, Supervision, Validation, Writing – Review & Editing.

## PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

## REFERENCES

[1] S. Kjaer, J. Pedersen, F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules", *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1292–1306, 2005, doi:10.1109/TIA.2005.853371.

[2] S. Mohammad Noor, A. Omar, N. Mahzan, I. Ibrahim, "A review of single-phase single stage inverter topologies for photovoltaic system", *in 2013 IEEE 4th Control and System Graduate Research Colloquium*, pp. 69–74, 2013, doi:10.1109/ICSGRC.2013.6653278.

[3] J. Jana, H. Saha, K. Das Bhattacharya, "A review of inverter topologies for single-phase grid-connected photovoltaic systems", *Renewable and Sustainable Energy Reviews*, vol. 72, pp. 1256–1270, 2017, doi:10.1016/j.rser.2016.10.049, URL: https://www.sciencedirect.com/science/.

[4] Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau, T. Shimizu, "Topologies of single-phase inverters for small distributed power generators: an overview", *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1305–1314, 2004, doi:10.1109/TPEL.2004.833460.

[5] K. R. Jardan, S. Dewan, G. R. Slemon, "General analysis of three-phase inverters", *IEEE Transactions on Industry and General Applications*, , no. 6, pp. 672–679, 1969, doi:10.1109/TIGA.1969.4181092.

[6] K. Sayed, A. Almutairi, N. Albagami, O. Alrumayh, A. G. Abo-Khalil, H. Saleeb, "A review of DC-AC converters for electric vehicle applications", *Energies*, vol. 15, no. 3, p. 1241, 2022, doi:10.3390/en15031241.

[7] Z. Zeng, H. Yang, R. Zhao, C. Cheng, "Topologies and control strategies of multi-functional grid-connected inverters for power quality enhancement: A comprehensive review", *Renewable and Sustainable Energy Reviews*, vol. 24, pp. 223–270, 2013, doi:10.1016/j.rser.2013.03.033.

[8] N. Mittal, B. Singh, S. Singh, R. Dixit, D. Kumar, "Multilevel inverters: A literature survey on topologies and control strategies", *in 2012 2nd International Conference on Power, Control and Embedded Systems*, pp. 1–11, 2012, doi:10.1109/ICPCES.2012.6508041.

[9] M. Vijeh, M. Rezanejad, E. Samadaei, K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view", *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9479–9502, 2019, doi:10.1109/TPEL.2018.2890649.

[10] J. Reimers, L. Dorn-Gomba, C. Mak, A. Emadi, "Automotive Traction Inverters: Current Status and Future Trends", *IEEE Transactions on Vehicular Technology*, vol. 68, no. 4, pp. 3337–3350, 2019, doi:10.1109/TVT.2019.2897899.

[11] M. A. Abusara, S. M. Sharkh, "Design and Control of a Grid-Connected Interleaved Inverter", *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 748–764, 2013, doi:10.1109/TPEL.2012.2201505.

[12] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters", *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1175–1189, 2008, doi:10.1109/TIE.2007.907671.

[13] O. Hegazy, J. Van Mierlo, P. Lataire, "Analysis, modeling, and implementation of a multidevice interleaved DC/DC converter for fuel cell hybrid electric vehicles", *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4445–4458, 2012, doi:10.1109/TPEL.2012.2183148.

[14] K. Tytelmaier, O. Husev, O. Veligorskyi, R. Yershov, "A review of non-isolated bidirectional dc-dc converters for energy storage systems", *in 2016 II International Young Scientists Forum on Applied Physics and Engineering (YSF)*, pp. 22–28, 2016, doi:10.1109/YSF.2016.7753752.

[15] R. R. De Melo, F. L. Tofoli, S. Daher, F. L. M. Antunes, "Interleaved bidirectional DC-DC converter for electric vehicle applications based on multiple energy storage devices", *Electrical Engineering*, vol. 102, no. 4, pp. 2011–2023, 2020, doi:10.1007/s00202-020-01009-3.

[16] O. Garcia, P. Zumel, A. De Castro, A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages", *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 578–586, 2006, doi:10.1109/TPEL.2006.872379.

[17] Y. Du, X. Zhou, S. Bai, S. Lukic, A. Huang, "Review of non-isolated bi-directional DC-DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks", *in 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1145–1151, 2010, doi:10.1109/APEC.2010.5433359.

[18] P.-L. Wong, P. Xu, P. Yang, F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors", *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 499–507, 2001, doi:10.1109/63.931059.

[19] J.-P. Lee, H. Cha, D. Shin, K.-J. Lee, D.-W. Yoo, J.-Y. Yoo, "Analysis and design of coupled inductors for two-phase interleaved DC-DC converters", *Journal of Power Electronics*, vol. 13, no. 3, pp. 339–348, 2013, doi:10.6113/JPE.2013.13.3.339.

[20] L. Ni, D. J. Patterson, J. L. Hudgins, "High power current sensorless bidirectional 16-phase interleaved DC-DC converter for hybrid vehicle application", *IEEE Transactions on Power electronics*, vol. 27, no. 3, pp. 1141–1151, 2011, doi:10.1109/TPEL.2011.2165297.

[21] M. Berrehil El Kattel, G. I. Carvalho Lobato, T. A. C. Maia, B. de Jesus Cardoso Filho, "99%—Efficient, interleaved bidirectional DC-DC converter with new interleaved PWM method of parallel-connected Mosfets", *International Journal of Circuit Theory and Applications*, vol. 50, no. 7, pp. 2439–2470, 2022, doi:10.1002/cta.3265.

[22] J.-C. Hwang, P.-C. Chen, C.-S. Liu, L.-R. Chen, "A novel single-phase interleaved Bi-directional inverter for grid-connection control", *in 2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, pp. 375–379, 2014, doi:10.1109/ISIE.2014.6864642.

[23] G. Gohil, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre, F. Blaabjerg, "Modified discontinuous PWM for size reduction of the circulating current filter in parallel interleaved converters", *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3457–3470, 2014, doi:10.1109/TPEL.2014.2339392.

[24] G. J. Capella, J. Pou, S. Ceballos, J. Zaragoza, V. G. Agelidis, "Current-balancing technique for interleaved voltage source inverters with magnetically coupled legs connected in parallel", *IEEE Transactions on Industrial Electronics*, vol. 62, no. 3, pp. 1335–1344, 2014, doi:10.1109/TIE.2014.2345345.

[25] R. Maheshwari, G. Gohil, L. Bede, S. Munk-Nielsen, "Analysis and modelling of circulating current in two parallel-connected inverters", *IET Power Electronics*, vol. 8, no. 7, pp. 1273–1283, 2015, doi:10.1049/iet-pel.2014.0656.

[26] J. Burkard, M. Pfister, J. Biela, "Control concept for parallel interleaved three-phase converters with decoupled balancing control", *in 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, pp. 1–9, 2018.

[27] S. A. D. Contreras, P. C. Cortizo, M. A. S. Mendes, "Simple control technique for interleaved inverters with magnetically coupled legs", *IET Power Electronics*, vol. 6, no. 2, pp. 353–363, 2013, doi:10.1049/iet-pel.2012.0514.

[28] V. H. M. Biajo, G. I. C. Lobato, S. M. Silva, "Analysis of a Novel High Power-Density Semiconductor-Level Interleaved Converter", *in 2023 IEEE 8th Southern Power Electronics Conference and 17th Brazilian Power Electronics Conference (SPEC/COBEP)*, pp. 1–8, 2023, doi:10.1109/SPEC56436.2023.10407546.

[29] L. K. M. Pereira, *et al.*, *Estudo da topologia, técnicas de modulação em largura de pulsos e controle do conversor boost entrelaçado*, Ph.D. thesis, Universidade Federal de Minas Gerais, 2019.

[30] N. Mohan, T. M. Undeland, W. P. Robbins, *Power electronics: converters, applications, and design*, John wiley & sons, 2003.

[31] A. Khoshkbar-Sadigh, V. Dargahi, K. Lakhera, K. Corzine, "Analytical design of LC filter inductance for two-level inverters based on maximum ripple current", *in IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, pp. 1621–1626, 2019, doi:10.1109/IECON.2019.8926919.

[32] K. Xing, F. C. Lee, D. Borojevic, Z. Ye, S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation", *IEEE Transactions on Power Electronics*, vol. 14, no. 5, pp. 906–917, 1999, doi:10.1109/63.788496.

[33] G. Gohil, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre, F. Blaabjerg, "Modified discontinuous PWM for size reduction of the circulating current filter in parallel interleaved converters", *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3457–3470, 2014, doi:10.1109/TPEL.2014.2339392.

[34] T. Wang, Z. Ye, G. Sinha, X. Yuan, "Output filter design for a grid-interconnected three-phase inverter", *in IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, vol. 2, pp. 779–784, 2003, doi:10.1109/PESC.2003.1218154.

[35] M. A. Abusara, S. M. Sharkh, "Design and Control of a Grid-Connected Interleaved Inverter", *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 748–764, 2013, doi:10.1109/TPEL.2012.2201505.

## BIOGRAPHIES

**Vítor H. M. Biajo** received his bachelor's degree in Electrical Engineering in 2020 and his master's degree in Electrical Engineering with an emphasis on Power Electronics in 2024 from the Federal University of Minas Gerais, Belo Horizonte, Brazil. He also studied Electrical Engineering and Sustainable Development at the École Supérieure d'Ingénieurs en Électrotechnique et Électronique d'Amiens, in France. Vítor has experience in powertrain controls and power electronics systems integration applied to electrification technologies. He is currently an Electric Propulsion Engineer at Eve Air Mobility, an Embraer company.

**Gideon I. C. Lobato** received the B.S. degree in electrical engineering from the Centro Federal de Educação Tecnológica de Minas Gerais, Belo Horizonte, MG, in 2009, and the M.S. degree in electrical engineering from the Universidade Federal de Minas Gerais (UFMG), Belo Horizonte, MG, in 2015, where he is currently working toward the Ph.D. degree in electrical engineering. He is currently a lead power electronics engineer at GE Power Conversion, Pittsburgh-US. His research interests include applications of power electronics in electric power systems, energy conversion, power quality analysis and enhancement, and renewable energy.

**Sidelmo M. Silva** received the graduation degree in electrical engineering (with a gold medal for the highest GPA), and the master's and Doctoral degrees in electrical engineering from the Federal University of Minas Gerais (UFMG), Belo Horizonte, Brazil, in 1997, 1999, and 2003, respectively. From 2001 to 2002, he was with the Development Department of ABB Switzerland, Turgi, as a System and Controls Engineer. From 2017 to 2018, he was a Visiting Scholar with the University of Wisconsin-Madison, Madison, WI, USA, where he was with microgrids. He is currently a full Professor with the Department of Electrical Engineering, Federal University of Minas Gerais. His research interests include power quality, applications of power electronics in electric power systems, microgrids, and renewable energy Generation.