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Grid-Forming Fuel Cell System for an Islanded AC Grid

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ABSTRACT This paper proposes a two-stage converter that can black start an isolated AC Microgrid with a Fuel Cell (FC) as the primary energy source. The first stage is connected to the FC and employs a Three-Leg Interleaved Boost DC/DC Converter (IBC), while the second is a Three-Phase Voltage Source Converter (VSC). The DC/DC stage utilizes a Cascade Voltage Control (CVC) to mitigate voltage fluctuations in the DC-link caused by the variability of the FC voltage. For the DC/AC stage, three distinct grid-forming (GFM) strategies are implemented with two of them with multi-loop cascaded structure and one with a single-loop structure. The power circuit of the system is simulated using the Real-Time Simulator (RTS) HIL 602+ from Typhoon-HIL, with the control strategies embedded on the Digital Signal Processor (DSP) TMS320F28379D - F28379D LaunchPad from Texas Instruments (TI). The performance of the cases are verified through CHIL simulations for a balanced and unbalanced inductive load steps. The results demonstrate that for both tests the GFM single loop structure presents smoother transients and shorter recovery times. Additionally, for the unbalanced loads, all the cases present similar results for the DC variables with more pronounced differences at the AC side.

KEYWORDS Grid-Forming, Fuel Cell, Voltage-Source Converter, Hardware-in-the-Loop

I. INTRODUCTION

Energy consumption has historically heavily relied on fossil fuels, contributing to climate change [1]. Depletion of these finite resources has driven exploration into alternative energy sources like solar, wind, hydroelectric, and geothermal energies [2]. Fuel Cells (FCs) are gaining attention due to their higher energy density and environmentally sustainable fuel transformation processes [2]. FCs are devices designed to directly convert the chemical energy of various fuels, including those from renewable sources, into electrical energy. These devices are also silent in operation [3].

The power and energy efficiency of an FC heavily rely on several factors, including thermodynamics, electrode kinetics, and reactant mass transfer [4]–[7]. Additionally, the choice of materials and components used in an FC significantly impacts its performance [8], remaining as the primary challenges in FC research and development.

Another area of research that has gathered significant interest is FC power conditioning [9]–[11]. FCs supply direct current (DC) at a low voltage and are typically connected to electric power networks through power conditioning units. Power electronic systems play a crucial role in ensuring that the FC´s electrical output is compatible with a wide range of loads by utilizing DC/DC and DC/AC converters. These converters facilitate the conversion of unregulated DC voltage into controlled DC or AC power, tailored to specific applications [12].

To adapt the output voltage of each FC array to the DC bus voltage, a DC/DC boost converter is employed, followed by a filter and an inverter (DC/AC converter) [13]–[17]. However, one of the challenges for the design of the boost converter is the high voltage gain demanded by the FC. Some strategies regarding this challenge have been developed, as the implementation of a differential connection between basic converters [18] and multi-phasing or interleaved converters [19].In fuel cell systems, interleaved boost converters (IBC) stand out by delivering high gain while minimizing current ripple, crucial to extend FC's lifetime and reduce the output capacitor [20].Also, the IBC reduces the filtering inductors, distributes current across each leg, and offers advantages like high efficiency, faster dynamics, and increased power density [21]. When considering the use of a FC in isolated systems, this power source can connect in grid-forming mode at the AC microgrid via a two-stage converter [22]–[24]. In [25], the design of a Controller Hardware-in-the-Loop (CHIL) configuration is described to test the integration of a FC storage system at an isolated AC microgrid. There, the integration consists of two stages: a three-leg Interleaved Boost Converter for the initial stage and a Voltage Source Converter (VSC) for the final stage.

The DC/DC stage employs Cascade Voltage Control (CVC), while for the DC/AC stage, three distinct GFM control strategies were tested. The first two contain a Multi-Loop structure [26], where the dq frame [27] is with Proportional-Integral (PI) controllers and the $\alpha\beta$ frame [28]

is with Proportional-Resonant (PR) controllers. Both multi-loop structures employ an inner current loop and an outer voltage loop. The last GFM strategy is a single-loop, the Synchronverter control [25], [29].

This work extend the validation of the converters and controls designed in [25] with some modifications and improvements, interpreted as the new contributions of the work and listed: i) this work proposes a novel topology for a converter that can use a FC system to black-start isolated loads, with both DC and AC models, which can encourage the development of control strategies for model-based design purposes; ii) the control strategies were validated for the detailed model of the FC, which incorporates the voltage drop in the activation region, iii) the system was tested for balanced and unbalanced loads scenarios, highlighting its limitations, which can help the further development of new control strategies to mitigate its impacts, iv) the control strategies were validated in the industry-grade Digital Signal Processor (DSP) TMS320F28379D - LaunchPad, through a CHIL simulation with the Real-Time Simulator (RTS) HIL 602+ provided by Typhoon-HIL.

The paper is structured as follows. The first section brings a brief state-of-art for FC applications in isolated systems. The second section describes the system converters and it's design. The third brings the FC model and the IBC modeling and control design. The fourth section presents the three implemented GFM controls and their design methodology and considerations. In the fifth section, the CHIL implementation is described with the results for the load connection tests. The sixth and final section presents the conclusions of this paper.

II. SYSTEM DESCRIPTION AND DESIGN

The power circuit of the system is shown in Figure 1 with its main three parts. The nominal parameters, based on [25], employed for designing the converters components are also shown in Table 1.

The first part is the FC model, described in section III, connected to the Interleaved Boost Converter (IBC), which utilizes a three-leg system comprising three inductors, each having an identical value and associated resistance, denoted as L_b and $R_{L,b}$ respectively. The measured leg currents are $i_{b,123}$. To ensure voltage stability at the output, a capacitor C_b is employed where its voltage is the control objective for the IBC and described in section III. C_b fulfills the dual role of boost's output capacitor and the VSC's input capacitor with no additional filtering. According to [30], the design of the IBC components can be carried out using with:

$$L_b = \frac{v_{out}(1-D)}{f_{sw,b}\Delta i_L i_{L,nom}}, \tag{1}$$

$$C_b = \frac{D}{f_{sw,b}R\Delta v_c N}, \tag{2}$$

where v_{out} is the IBC output voltage, D is the Duty Cycle of the IBC, $f_{sw,b}$ denotes the switching frequency of the converter, Δi_L represents the desired current ripple through the input inductors, Δv_c the desired voltage ripple, both under nominal load conditions, R stands for the resistance to reach nominal load, N the number of legs of the converter, and $i_{L,nom}$ is the load nominal current.

The relationship between the input and output voltages that calculate D is described by:

$$\frac{v_{out}}{V_{FC}} = \frac{1}{1-D}, \tag{3}$$

where V_{FC} stands for the FC voltage at nominal load. Both $i_{b,123}$ and v_{out} are fed back to the control system, which generates the Pulse Width Modulation (PWM) signals for the IBC.

The second stage comprises a two-level three-phase Voltage Source Converter (VSC) [27] with a damped low-pass LC filter.The design of the output inductor L_i, the capacitor C_{inv} and the damping resistance R_{damp} are described by:

$$L_i = \frac{v_{out}}{8\Delta i_{L,inv} I_{nom} f_{sw,inv}}, \tag{4}$$

$$C_i = \frac{1}{4L_i\pi^2 f_{res}^2}, \tag{5}$$

$$R_{damp} = \frac{1}{\omega_{nom} C_i q_f}, \tag{6}$$

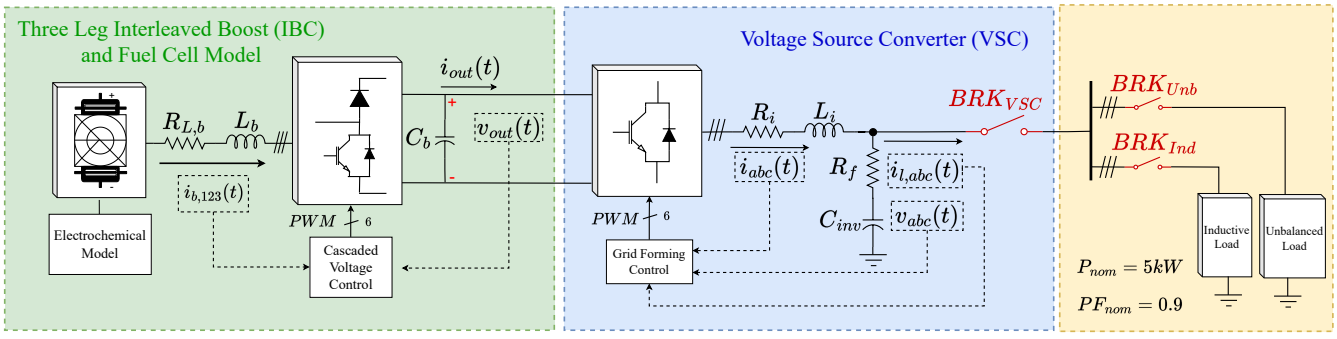

FIGURE 1. Two Stage Converter Circuit for FC integration.

TABLE 1. IBC and VSC Parameters.

P_{system} [kW]	$V_{\text{out,boost}}$ [V]	$\Delta i_{\text{L}_{\text{b,123}}}$ [%]	Δv_{out} [%]	$f_{\text{sw,b}}$ [kHz]	S_{inv} [kVA]	$v_{\text{abc,nom}}$ [V]	$f_{\text{sw,inv}}$ [kHz]	$\Delta i_{\text{L}_{\text{inv}}}$ [%]
5	440	10	0, 1	10	5/0.8	$\sqrt{2}$.127	10	10
$f_{\text{res,LC}}$ [kHz]	q_f [DV]	C_b [μ F]	L_b [mH]	$R_{L,b}$ [$m\Omega$]	L_i [mH]	R_f [mΩ]	R_{damp} [Ω]	C_i [μ F]
1	50	772.83	1,215	5	1.1856	4.5	2.483	21.3658

where $\Delta i_{L,inv}$ is the desired current ripple at nominal load, I_{nom}, and the switching frequency, $f_{sw,inv}$. The capacitor is designed for the desired resonance frequency f_{res}, which is typically set to be one-tenth of $f_{sw,inv}$. The damping resistance is designed using a dimensionless parameter q_f, which influences the quality of damping at nominal frequency ω_{nom}, in this work $2\pi 60$ rad/s.

The third stage is the load for which the VSC is responsible for supplying power. This work tests two scenarios of isolated loads. The first is a balanced inductive load of 5 kW and power factor of 0.9 and connected through a circuit breaker BRK_{Ind}. The second is an unbalanced inductive load with same phase power rating as the balanced load. The main difference is that the phase a load is not connected.

III. FUEL CELL AND INTERLEAVED BOOST CONVERTER

The Proton-exchange Membrane Fuel Cell (PEMFC) model is based on [31] and [32], focusing on describing the voltage losses, which are proportional to the energy drawn from the PEMFC. The most significant factors contributing to voltage drop include activation polarization, ohmic polarization, and concentration polarization.

According to [31], the polarization curve, $V(i)$ can be equated to voltage drops from the theoretical voltage by the principal voltage losses:

$$V(i) = V_{th} - v_{act} - v_{ohmic} - v_{conc}, \tag{7}$$

where V_{th} is the PEMFC theoretical voltage, v_{act} is the activation polarization, v_{ohmic} is the ohmic polarization and v_{conc} is the concentration polarization.

The activation overpotential equation describes the voltage loss needed to overcome the energy barrier for the electrochemical reaction:

$$v_{act} = \frac{RT}{\alpha F} \ln\left(\frac{i}{i_0}\right), \tag{8}$$

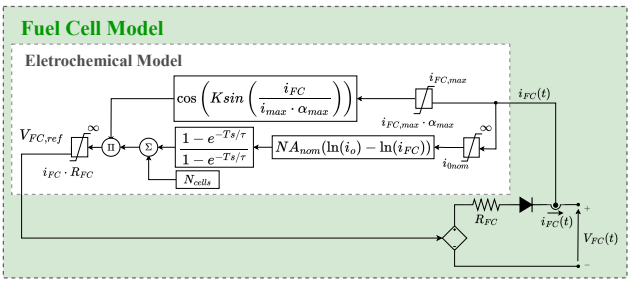

FIGURE 2. Circuit topology of the PEMFC.

where R is the ideal gas constant, T is the PEMFC temperature, α is the charge transfer coefficient, F is the Faraday's constant, i is the current density, and i_0 is the reaction exchange current density.

The ohmic losses are calculated using Ohm's law:

$$v_{ohmic} = R_{ohmic} i, \tag{9}$$

where R_{ohmic} is the total cell resistance and i is the current of the fuel cell.

The concentration losses are given by:

$$v_{conc} = \frac{RT}{nF} \ln\left(\frac{C_0}{C_i}\right), \tag{10}$$

n is the number of electrons transferred per mol of consumed reactant, C_0 is the concentration at the gas diffusion layer and C_i is the concentration at the catalyst layer interface.

Figure 2 shows the mathematical model implementation: considering that each cell has $V_{th} = 1\ V$, the maximum voltage reached by the PEMFC depends on the number of cells contained in the system. This voltage decreases according to the required current, as described in (8) and (9). Thus, the model provides a voltage reference for a controllable voltage source connected to the PEMFC resistance and a diode, ensuring unidirectionality. The model also includes a saturation mechanism for the PEMFC maximum current. To align with offline and RT tests, the PEMFC model was based on parameters from [32], as shown in Table 2. Using these parameters, the polarization and power curves of the PEMFC stack can be drawn as shown in Figure 3.

TABLE 2. PEM Fuel Cell modeling parameters.

Parameter	Description	Value
P_{FC}	Nominal Power	6 kW
$V_{FC,nom}$	Nominal operation voltage	45 V
i_0	Exchange current	0.2919 A
$i_{FC,max}$	Maximum operating current	227.25 A
α_{max}	Maximum exchange coefficient	0.99 A
R_{FC}	PEMFC resistance	0.0783 Ω
N_{cells}	Number of cells	65
$Ksin$	Saturation constant	155.5088
NA_{nom}	Cell dynamic constant	1.56 V
τ	Time constant	1 s
T	Response time	0.333 s

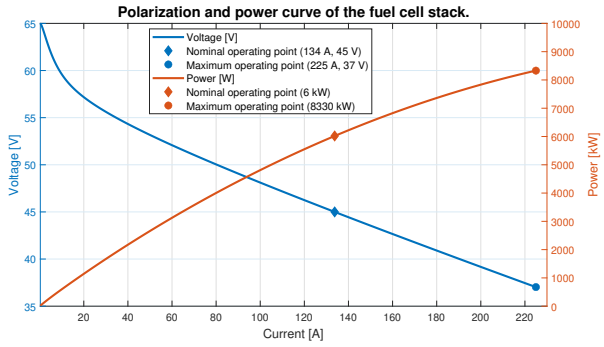

FIGURE 3. Polarization and power curve of the fuel cell stack.

To derive an average voltage model that describes the converter's operation, the circuit's model, as shown in Figure 1, follows the procedure presented in [30]. This model simplifies the system by treating each leg as if it contains a controlled voltage source. Here, d_n denotes the duty cycle associated with each leg:

$$\sum_{i=1}^{N} I_{b,n}(s) = C_b s V_{out}(s), \tag{11}$$

$$-d_n(s)V_{FC,ref} + [L_b s + R_{L,b}] \sum_{i=1}^{N} I_b(s) + N V_{out}(s) = 0. \tag{12}$$

As proposed in [30], assuming that $V_{FC,ref}$ is constant, the system under analysis is a Multiple-Input Multiple-Output (MIMO) system, where the outputs are the currents across the inductors, $I_{b,n}$, and the capacitor voltage, v_{out}, and the inputs are the duty cycles (d_n) and the load current, I_{out}. To analyze the influence of one input variable, the others need to be zero.

By manipulating (12), one can derive the transfer function that establishes the relationship between duty cycle and phase current:

$$\frac{I_{b,n}(s)}{D_n(s)} \approx \frac{V_{FC,ref}}{L_b s + R_{L,b}}. \tag{13}$$

Considering that all inductance values are identical, the following approximation can be made:

$$\frac{V_{out}(s)}{I_{boost,n}(s)} = \frac{N}{C_b s}. \tag{14}$$

The implemented control was adapted from [30] and the diagram is shown in Figure 4. It uses the same controller gains formula and methodology using a CVC with an outer loop controlling the output voltage, v_{out}, and an inner loop with three separate controllers controlling the current in each leg, $i_{b,n}$.

According to [30], the gains of the inner loop are calculated with normalized values with:

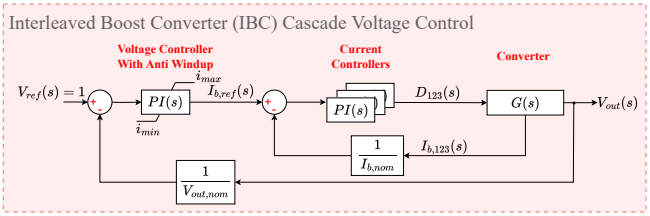

FIGURE 4. IBC Voltage Control diagram.

$$k_{p,I} = \frac{L_b \cdot P_{system}}{\tau_{i,boost} \cdot V_{FC,nom}^2}, \tag{15}$$

$$k_{i,I} = \frac{R_{L,b} \cdot P_{system}}{\tau_{i,boost} \cdot V_{FC,nom}^2}, \tag{16}$$

where $\tau_{i,boost}$ is the controller time constant and, $k_{p,I}$ and $k_{i,I}$ are coefficients representing the proportional and integral terms, respectively.

The gains of the outer loop are also calculated with normalized values and designed by the Symmetrical Optimum Method [33] with:

$$k_{p,V} = \frac{C_b \cdot v_{out}^2}{2a \cdot \tau_{i,boost} \cdot P_{system}}, \tag{17}$$

$$k_{i,V} = \frac{k_{p,V}}{a^2 \cdot \tau_{i,boost}}, \tag{18}$$

where $k_{p,V}$ and $k_{i,V}$ are coefficients representing the proportional and integral terms, respectively, $\tau_{i,boost}$ is the inner loop time constant, and a is the symmetrical optimum adjustment factor.

IV. GRID FORMING CONTROLS MODELLING AND ANALYSIS

To establish the AC grid, a three-phase two-level VSC was utilized, a well-established converter known for its control flexibility and straightforward implementation [27]. For supplying the isolated loads, the inverter employs GFM to operate as a voltage source, regulating both voltage and frequency supplied to the load, with a diagram of its generic structure shown in Figure 5.

This control philosophy does not rely on synchronization algorithms and operates with an internal phase reference. This is done by measuring both active power and reactive power provided to the load or the grid, P_{meas} and Q_{meas}, and calculated by:

$$P_{meas} = v_{d,\alpha} i_{d,\alpha} + v_{q,\beta} i_{q,\beta}, \tag{19}$$

$$Q_{meas} = v_{q,\beta} i_{d,\alpha} - v_{d,\alpha} i_{q,\beta}, \tag{20}$$

where $v_{d,\alpha}$ stands for the voltage calculated by the reference frame transformation aligned with the converters phase a, where depending on the transformation can be the direct axis voltage, v_d, or α axis voltage v_α. Following the same pattern, $v_{q,\beta}$ represents the transformations voltage which are

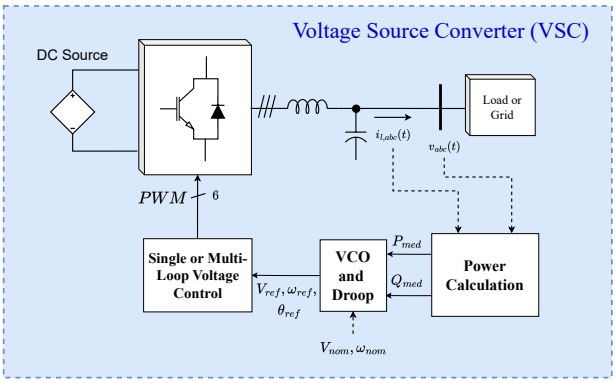

FIGURE 5. Grid-Forming Control generic structure.

90^o degrees behind a axis. The associated axis currents are $i_{d,\alpha}$ and $i_{q,\beta}$.

The power measurement is sent to the Voltage Controlled Oscillator (VCO), associated with voltage and frequency droops. According to [34], the VCO and Droop block uses the converter's rated voltage V_{nom} and frequency ω_{nom} to calculate the controls voltage references of amplitude V_{ref}, frequency, ω_{ref}, and phase, θ_{ref}, with:

$$\omega_{ref} = \omega_{nom} - \frac{1}{D_p}\frac{1}{\tau_{filter}+1}P_{meas}, \tag{21}$$

$$V_{ref} = V_{nom} - \frac{1}{D_q}\frac{1}{\tau_{filter}+1}Q_{meas}, \tag{22}$$

$$\theta_{ref} = \frac{1}{s}\omega_{ref}, \tag{23}$$

where D_p is the frequency droop, D_q the voltage droop and τ_{filter} is the time constant of a low-pass filter that depending on the employed voltage control can help to stabilize the control with a cost of slowing the response time. The references are finally sent to the voltage control which can use a single-loop, directly generating the reference for the PWM strategy, or a multi-loop structure with the well established cascaded structures [26].

In this study, three GFM control strategies were implemented and evaluated: the first adopts a multi-loop structure in the dq frame with PI controllers, the second a multi-loop structure in the $\alpha\beta$ frame with PR controllers, and the third a single-loop structure known as Synchronverter concept (SC), emulating the operation of a synchronous generator (SG).

A. Synchronous reference frame cascaded control

The design of this control follows similar steps as for the IBC, with an inner loop controlling the inverters currents, i_{abc}, and an outer loop controlling the output voltage, v_{abc}, [27]. The inner loop transfer function with normalized values is described by:

$$\frac{I_{dq}(s)}{V_t(s)} = \frac{Z_{ac,inv}}{L_i s + R_i}, \tag{24}$$

$$Z_{ac,inv} = \frac{v_{abc,nom}}{I_{nom}}, \tag{25}$$

where V_t is the terminal voltage generated by the PWM strategy, I_{dq} are the direct and quadrature currents that flow through inductors L_i and $Z_{ac,inv}$, the base impedance, also known as the converter gain. With this TF, the PI controllers can be designed by means of a desired response time for the closed loop system $\tau_{i,inv}$ by the following equations:

$$k_{p,I} = \frac{L_i}{\tau_{i,inv}\cdot Z_{ac,inv}}, \tag{26}$$

$$k_{i,I} = \frac{R_i}{\tau_{i,inv}\cdot Z_{ac,inv}}. \tag{27}$$

For the outer loop, the normalized TF that relates the output voltage V_{dq} with the inner loop currents I_{dq} can be described by:

$$\frac{V_{dq}(s)}{I_{dq}(s)} = \frac{1}{Z_{ac,inv}C_i s}. \tag{28}$$

For this loop the controller must be able to control a second order plant composed by the equivalent inner loop and (28) cascaded with the PI controller. This can be done by the Symmetrical Optimum Method [33], with the normalized gains calculated by the following equations:

$$k_{p,V} = \frac{C_{inv}\cdot Z_{ca,inv}}{a\cdot\tau_{i,inv}}, \tag{29}$$

$$k_{i,V} = \frac{k_{p,V}}{a^2\cdot\tau_{i,inv}}, \tag{30}$$

where a is the adjustment factor chosen as 2 for disturbance rejection [33]. Figure 6 shows the implemented diagram where the control receives the reference voltages, $V_{dq,ref}$, calculated using the VCO's references. The inner loop reference is limited for current limitation purposes and receives as feedback the converters output current I_{dq} and the load current $I_{L,dq}$.

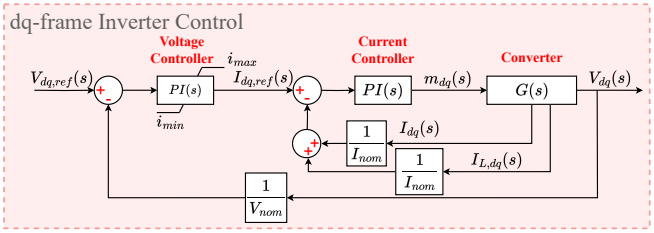

FIGURE 6. dq-frame Inverter control diagram.

For this control, $\tau_{i,inv} = 500\ \mu s$ and $a = 1.4$ were chosen and the controllers gains are shown in Table 4.

B. Stationary reference frame cascaded control

The second control strategy is presented in [28], and is a methodology to adapt the design of *PI* controllers in the *dq* frame to *PR* controllers in the $\alpha\beta$ Frame. The controller is designed to have a high gain at the desired frequency. The controller transfer functions are described by:

$$PI(s) = k_p + \frac{k_i}{s}, \tag{31}$$

$$PR(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_r^2}, \tag{32}$$

where k_p are the proportionals gains, k_i the PI's integral gain, k_r the resonant gain of the PR, and ω_c is a constant that smooths the resonant gain and increases the bandwidth of the controller. The *PR* gains adaptation based on the *PI* can be calculated by:

$$k_{p,PR} = k_{p,PI}, \tag{33}$$

$$k_{r,PR} = 2 \cdot k_{i,PI}. \tag{34}$$

The proportional gains are equal and k_r is the double of k_i ensuring a faster response with lower bandwidth [28]. The control diagram is shown in Figure 7 with similar cascaded structure implemented in the *dq* frame with the following differences: 1) The inner loop current reference does not present a limitation for overcurrent protection, and 2) the $\alpha\beta$-frame does not need extra measuring from the load currents to decouple the axis [27]. The $\alpha\beta$-frame controllers gains $k_{p,I}$, $k_{r,I}$, inner loop, $k_{p,V}$, $k_{r,V}$, outer loop, values are shown in Appendix A.

C. Synchronverter control

The last GFM control is the Synchronverter concept (SC) [29], based on a simple model of a SG to control a power converter and take advantage of properties as Synthetic Inertia and Voltage Regulation. Different from a conventional SG, the Synchronverter is more flexible as its inertia and excitation system are emulated through the control algorithm and not directly related to physical devices. This model is derived from the Swing Equation of the SG (35) to calculate the internal frequency:

$$\dot{\omega} = \frac{1}{2H}[-T_e - D_p(\omega - \omega_{ref})], \tag{35}$$

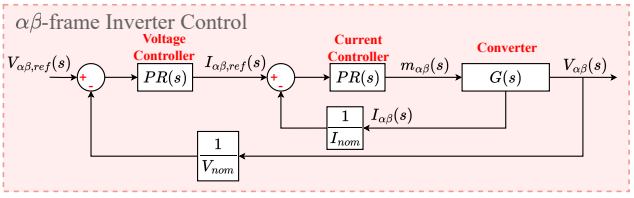

FIGURE 7. $\alpha\beta$ **Inverter control diagram.**

where the converters frequency, ω, is calculated from, T_e, the electromagnetic torque equivalent to the load power and the frequency droop gain, represented by D_p. H is the inertia constant of the virtual machine. The excitation system is described by:

$$M_f i_f = \frac{1}{K}\int [Q_{ref} - Q - D_q(V_{ref} - V_{pcc})]\, dt, \tag{36}$$

$$V_{pcc} = \sqrt{(V_\alpha^2 + V_\beta^2)}, \tag{37}$$

where $M_f i_f$ is the magnetic flux, a function of K, the excitation gain, Q_{ref} forced to zero in island mode, Q, the supplied reactive power and the contribution of the voltage droop, calculated with D_q, the reference voltage V_{ref}, and V_{pcc} is the measured voltage amplitude. The equations to calculate T_e, Q and the modulation signals are implemented in the $\alpha\beta$-frame [35] and described by:

$$T_e = \frac{e_\alpha i_\alpha + e_\beta i_\beta}{\omega}, \tag{38}$$

$$Q = v_\beta i_\alpha - v_\alpha i_\beta, \tag{39}$$

$$\mathbf{e}_{\alpha\beta} = \omega M_f i_f \begin{bmatrix} sin\theta \\ -cos\theta \end{bmatrix}. \tag{40}$$

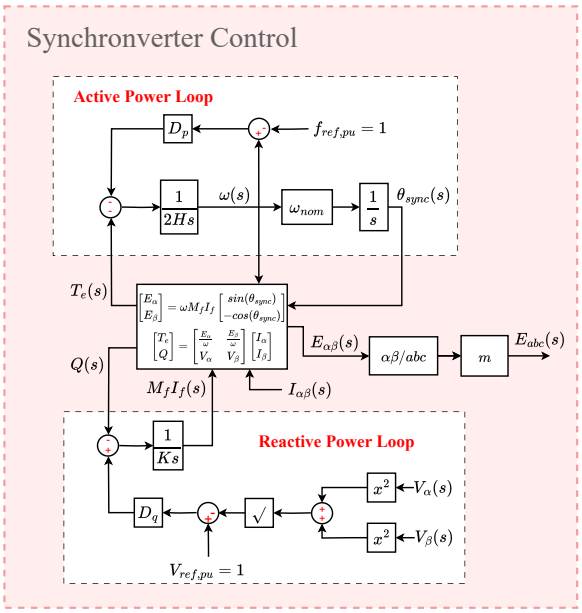

FIGURE 8. Synchronverter control diagram.

The normalized control diagram of the SC is shown in Figure 8. In contrast to the multi-loop structure, the Synchronverter incorporates both power calculation block and voltage control loop in the block in the middle of the diagram. The VCO is represented by the Active Power Loop (APL), at the top, and the Reactive Power Loop (RPL), at the bottom. Both APL and RPL have an integral part in parallel with a droop constant, generating a first order response [36], commonly with no need to implement low

pass-filters after calculating T_e and Q. Additionally, the APL and RPL are used to calculate the VCO's references and in parallel to Figure 5, ω stands for ω_{ref}, θ_{sync} for θ_{ref} and $E_{\alpha\beta}$ for V_{ref}. Finally, the control calculates the voltage reference for the PWM strategy E_{abc} after passing through the gain m, representing the VSC rated modulation factor.

The controllers gains $2H$ and K can be adjusted as functions of the Droop Constants and desired response times for the respective control loops. The APL time constant, τ_f, and RPL time constant, τ_v, are related to the controllers gains $2H$ and K by the following equations:

$$2H = \tau_f D_p, \text{ where: } D_p = \frac{\Delta P}{\Delta \omega}, \tag{41}$$

$$K = \tau_v D_q, \text{ where: } D_q = \frac{\Delta Q}{\Delta V}. \tag{42}$$

For this work the control gains are reproduced from [29] and τ_f and τ_v are chosen as 10 ms. The droop constants D_p and D_q are chosen as 50 and implemented in all the GFM structures. The controllers gains $2H$ and K are shown in Table 5.

V. HARDWARE-IN-THE-LOOP TESTS

A. Test bench and simulation workflow

To assess the effectiveness of the control strategies, the power structure configuration shown in Figure 1, is emulated in the RTS HIL 602+. The control strategies are embedded in the DSP TMS320F28379D with Matlab's Embedded Coder library. Figure 9 shows the CHIL setup employed to acquire the experimental results.

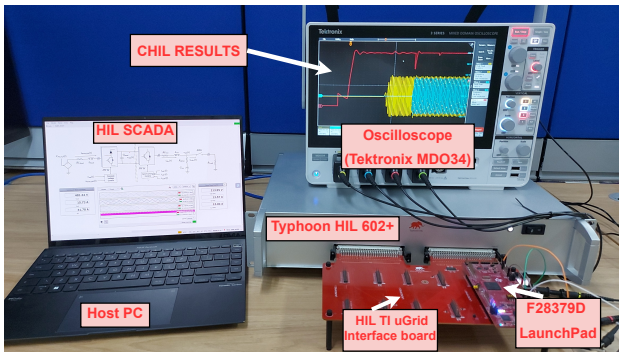

FIGURE 9. CHIL setup utilized to obtain the experimental results.

The two tested loads shown in Figure 1 are connected and the electrical measurements of the system are exported through the RTS software and post-processed in Matlab. The sample rate of the exported signals is equal to the simulation time step, 5 μs, and the control algorithms run at a 50 μs sample time.

For both tests the simulation workflow is structured as follows: first, the IBC is initialized, and the control tracks the output voltage reference; second, the VSC is initialized, ramping up the AC voltage reference signal; third, there is a 3 seconds interval for the controls reach steady-state; and finally, the respective load is connected.

B. Inductive load connection

Figure 10 shows the IBC output voltage, v_{out}, considering each inverter control for the inductive nominal load connected at approximately $t = 0.3$ s. For all the cases, before the load connection and with the VSC operating, v_{out} is controlled at 1 $p.u.$ After the load connection, there is a sudden drop in v_{out}. When using the $\alpha\beta$ frame control, the amplitude of $v_{out}(t)$ (shown by the blue curve) decreases to around 0.6 $p.u.$ and then returns to 1 $p.u.$ only after 1.6 seconds. As expected, the combination of the proportional and resonant control actions presented a faster response, rather than the proportional and integral combination, leading to the discharge of capacitor C_b. Although the control remains stable, there is no power available to be delivered by the FC that can charge the capacitor and continuously supply the load. With respect to capacitors safety limits, undervoltage is not a concern, but the VSC converter will overmodulate and not be able to ensure the load supply safely.

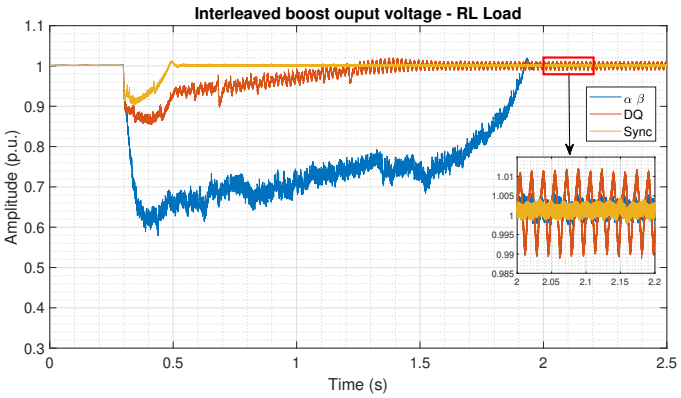

FIGURE 10. Response of $v_{out}(t)$ in RT Simulations for the inductive Load Connection.

When employing the dq frame control, the amplitude of $v_{out}(t)$ (shown by the red curve) drops to about 0.85 $p.u.$ and returns to 1 $p.u.$ after around 1 second. For this control, there is also a considerable transient before v_{out} returns to the nominal value. For the SC, the amplitude of $v_{out}(t)$ (indicated by the orange curve) shows the best result decreasing to around 0.9 $p.u.$ and returning to 1 $p.u.$ after 0.2 seconds. Lastly, when the controls reach steady state, a zoom is applied to improve visualization. For the $\alpha\beta$ and SC curves, v_{out} remains stable along with the desired voltage ripple, though for the dq control there is an oscillation measured in around 60 Hz, indicating an interaction between the AC and DC sides of the system, common when the impedance of the capacitor in the dc-link is not high enough to decouple the converter's sides. Although all cases employ the same control for the IBC, there is a notable difference between the cases, for both the load connection transient and steady-state as each controller also presents a different response.

Figure 11 shows the difference in the response of the AC variables, respectively, VSC's capacitor voltage and the load current (after the LC filter). When $\alpha\beta$ frame control is

employed, the effects of the DC undervoltage are highlighted with the voltage and current presenting a distortion with a third harmonic profile indicating that the converter is over-modulated. Also, before the load connection, the amplitude of the voltage is above 1 *p.u.*, indicating that the adaption to the PR controller is not fully tuned to control the VSC's output voltage and should be adjusted.

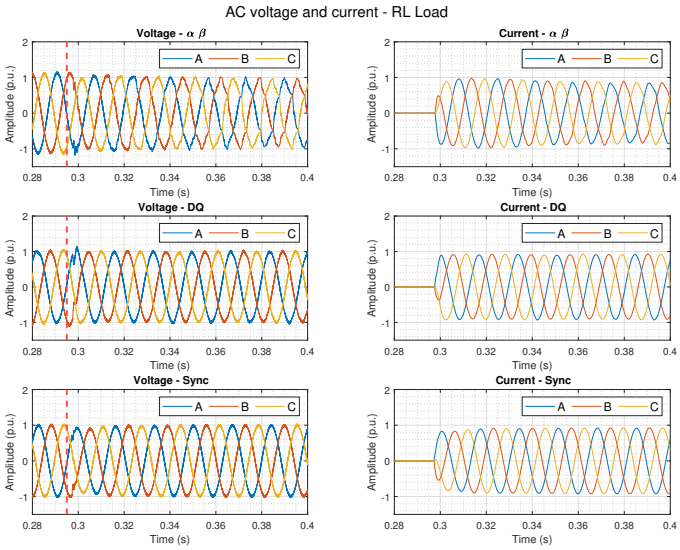

FIGURE 11. Response of AC voltage and current in RT Simulations for the inductive Load Connection.

For both *dq* frame and SC, before the load connection, the controls are able to maintain the voltage amplitude near 1 *p.u.* and after the load connection, there is a transitory that for both cases lasts less than a cycle. As the controls reach steady state, it is shown that the currents are around 0.9 *p.u.*, since the load power is lower than the converters capacity, there is still a conduction margin for the converter. For both cases the voltage and current remained with a sinusoidal profile.

As the last result, Figure 12 shows the voltage and current drawn from the fuel cell when the load is connected. Initially, the FC's voltage is around 1.35 *p.u.* as the no-load voltage is higher than at nominal load. After the connection of the load, represented by the red dashed line, the FC experiences a delay before increasing its current and decreasing the voltage. This delay can help to understand the undervoltage at v_{out}. Before the increase of the FC current there is an energy imbalance that causes the discharge of the capacitor and can only be compensated after the response of the FC.

When the load connects, the current is ramped and for all the cases there are oscillations caused by the interaction between the IBC switching and the FC model. The FC's voltage depends directly of its current propagating the switching effects in the converter. For the $\alpha\beta$ control the oscillations presents a higher amplitude compared to the *dq* and Sync controls. Meanwhile, after the load connection, the controls remain stable. At the end of Figure 12 it is shown that the

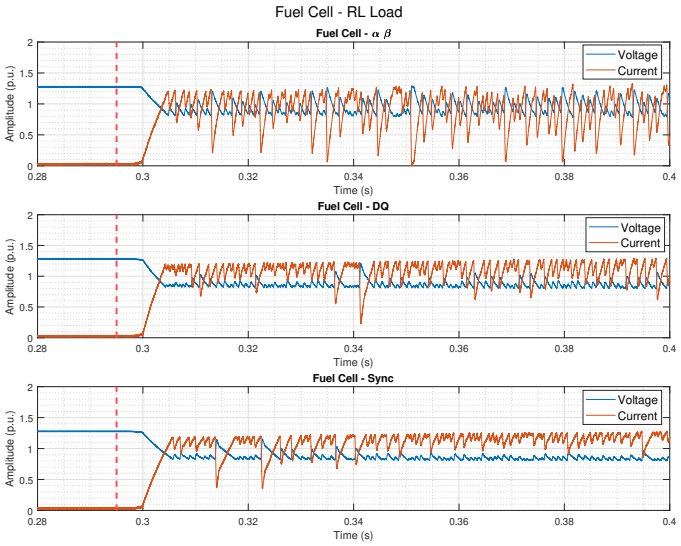

FIGURE 12. Response of Fuel Cell voltage and current in RT Simulations for the inductive Load Connection.

current from the sync control has a lower amplitude in the oscillation compared to the *dq* control.

C. Unbalanced load connection

For the unbalanced load test, the set of variables presented for the balanced load test are repeated. Figure 13 shows the IBC output voltage considering each inverter control around the load connection, at $t = 0.95$ *s*. Before the connection, all cases control v_{out} at 1 *p.u.* and after the connection there is a drop to approximately 0.94 *p.u.* followed by the recovery in about 200 *ms*. Despite the load connection presents the same per phase rating as the three phase balanced load, the drops in v_{out} are not as significant as for the balanced load.

Immediately after the connection, v_{out} presents an oscillation measured in $2\pi 119$ Hz, lower than twice the nominal frequency due to the implemented frequency droop. These oscillations are expected for unbalanced loads and presented almost the same amplitude for all three cases with the $\alpha\beta$ presenting the higher amplitude.

Figure 14 shows the VSC's three phase voltage and currents. For the $\alpha\beta$ and sync controls the voltage remains with a sinusoidal profile with the $\alpha\beta$ presenting the most pronounced unbalancing, after the load connection. For both

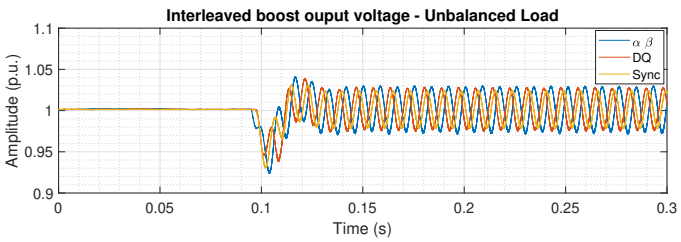

FIGURE 13. Response of $v_{out}(t)$ in RT Simulations for the unbalanced Load Connection.

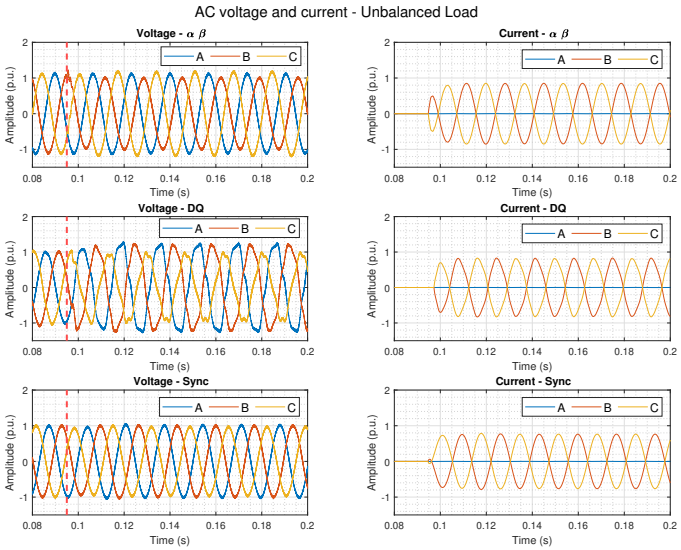

FIGURE 14. Response of AC voltage and current in RT Simulations for the unbalanced Load Connection.

cases, current remains with a sinusoidal profile with the same amplitude.

For the *dq* control the voltage presents a remarkable distortion indicating that the control design is not able to track the reference, even with some unbalance, after the load connection. This distortion is propagated for the current, which does not remain sinusoidal and would not be able to supply the load within safety limits.

Figure 15 shows the results for the FC's voltage and current. After the load connection, the FC response time is causing a delay before the current increases. After the connection, the oscillation of double fundamental frequency is propagated to the FC's voltage and current for all cases. As the voltage from the FC depends on the current level, this

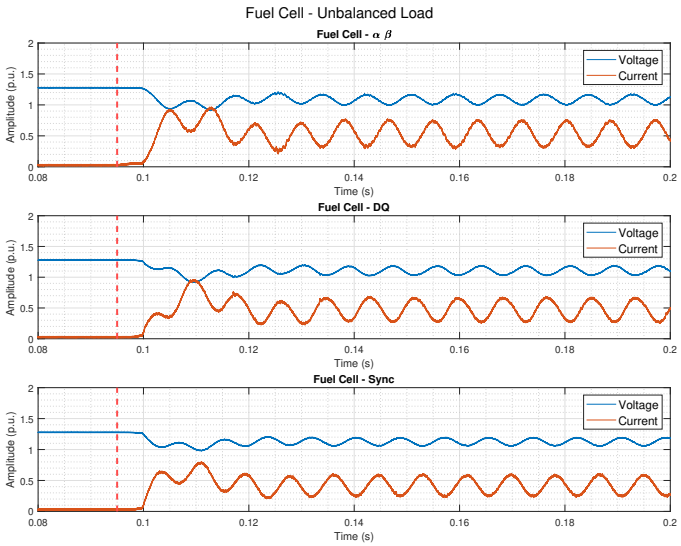

FIGURE 15. Response of Fuel Cell voltage and current in RT Simulations for the unbalanced Load Connection.

oscillation could be amplified as a resonance and damage the FC. Despite this oscillation, all the controls were able to remain stable, even for the *dq* control, where the AC variables are not within the expected sinusoidal profile.

D. Voltage THD and unbalance

Table 3 shows the Total Harmonic Distortion (THD) and unbalance results (in %) for the AC voltage of all three controllers with inductive and unbalanced loads.

TABLE 3. Voltage THD and Unbalance.

Controller	Inductive Load		Unbalanced Load	
	THD	Unbalance	THD	Unbalance
$\alpha\beta$	8.35 %	0.25 %	4.32 %	8.21 %
dq	7.30 %	1.53 %	9.84 %	18.26 %
Sync	6.03 %	1.17 %	4.94 %	3.92 %

For the inductive load, the $\alpha\beta$ controller presents the worst results for voltage THD, about 8.35%, compared with dq and SC controllers, with THDs of 7.30% and 6.03%, respectively. The unbalance in voltages for inductive loads is small for all controllers, at approximately 0.25%, 1.53%, and 1.17% for $\alpha\beta$, DQ, and SC, respectively. For unbalanced loads, the DQ controller shows the worst results for voltage THD at 9.84% and unbalance in voltage at 18.26%, compared to 4.32% and 8.21% for the $\alpha\beta$ controller, and 4.94% and 3.92% for the SC controller. When comparing controller performance for different load connections, the SC controller presents the best behavior for voltage THD and unbalance.

VI. CONCLUSION

This paper presents the modeling and control design of a two-stage converter to form an isolated AC grid using a FC system as a primary energy source. The first stage is a three-leg Interleaved Boost Converter (IBC) and the second is a Voltage Source Converter (VSC). For the VSC, three Grid-Forming strategies were implemented following the guidelines found in literature. The control algorithms were tested in a microcontroller interfaced with a Real Time Simulator using the Controller Hardware-in-the-Loop (CHIL) methodology. To assess the limitation of each control design, two tests were performed: connecting a balanced and unbalanced resistive/inductive load.

The results show that for the balanced load the $\alpha\beta$ control presents a pronounced undervoltage in the DC-link, caused by the resonant part of the controller, which could be a risk to supply the load in an acceptable power quality limit as the converter operates in overmodulation. The FC results show that the interaction of the converter switching and the model of the FC can propagate oscillations through the converter, which can be avoided using storage systems, such as supercapacitors, at the FC output. For the unbalanced load, the *dq* control presents the more distorted results for the AC voltage and is not indicated for this type of load without any modification in the control. The oscillations caused by the

unbalanced load are propagated through the converter to the FC. Although there are not any instability issues, the effects of these oscillations in the FC should be further analyzed. For the implemented controls, only the Synchronverter, which employs a single-loop structure, was able to maintain AC and DC variables in acceptable values for both cases.

For future work, the detailed small-signal modeling of the system, considering both power circuit and control, could be implemented to investigate the interaction between the IBC and FC. Thus, the controllers could be better tuned and present a response that minimizes this interaction. Additionally, the incorporation of the grid-connected mode could be implemented to assess the performance of the controllers within an electrical grid. Finally, imbalance compensation strategies can be investigated to improve the response of the controls.

Appendix

Table 4 and Table 5 shows the controllers gains for all implemented cases. The values of D_p and D_q were fixed at 50 for all cases. For the Synchronverter no low-pass filter was used after calculating the powers provided by the converter.

TABLE 4. dq**- frame and** $\alpha\beta$ **Controllers Parameters.**

dq frame Controller		$\alpha\beta$ Controller	
Parameter	Value	Parameter	Value
$k_{p,I}$	0.6124 $p.u.$	$k_{p,I}$	0.6124 $p.u.$
$k_{i,I}$	2.5669 $p.u.$	$k_{r,I}$	5.1338 $p.u.$
$k_{p,V}$	0.2340 $p.u.$	$k_{p,V}$	0.2340 $p.u.$
$k_{i,V}$	935.9650 $p.u.$	$k_{r,V}$	1871.92 $p.u.$
τ_{filter}	10 ms	ω_c	$5/2\pi 60$ rad/s
		τ_{filter}	10 ms

TABLE 5. Synchronverter Controllers Parameters.

Synchronverter Controller	
Parameter	Value (p.u.)
$2H$	0.5 $p.u.$
K	0.5 $p.u.$
τ_{filter}	10 ms

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AUTHOR'S CONTRIBUTIONS

J. M. T. AMARAL: Conceptualization, Formal Analysis, Investigation, Methodology, Project Administration, Software, Supervision, Validation, Writing – Review & Editing. **J. S. RAMOS:** Data Curation, Investigation, Software, Validation, Writing – Original Draft. **C. C. M. SOUZA:** Data Curation, Investigation, Validation, Writing – Original Draft. G. J. DA SILVA: Data Curation, Investigation, Validation, Writing – Original Draft. **E. L. V. EMMERIK:** Formal Analysis, Methodology, Supervision, Writing – Review & Editing. **R. F. S. DIAS:** Funding Acquisition, Resources.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

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