



Received July 30, 2024; accepted December 29, 2024; Date of publication January 22, 2025. The review [o](https://orcid.org/0000-0001-5969-720X)f this paper was arranged by Associate Editor Francisco D[.](https://orcid.org/0000-0003-0710-7815) Freijedo<sup>o</sup> and Editor-in-Chief Heverton A. Pereira<sup>®</sup>. *Digital Object Identifier<http://doi.org/10.18618/REP.e202510>*

# **Thermoelectric Characterization of IGBT Power Modules: An Approach by Static and Dynamic Methods**

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**ABSTRACT** This study evaluates IGBT modules with a focus on efficiently measuring their thermal impedance, a critical factor in reliability assessments. The research employs the Thermo Electric Sensitive Parameter method to measure the Virtual Junction Temperature and obtain the Thermal Impedance curve. These experimental results are compared with datasheet values, using power modules without a baseplate. Two methodologies, dynamic and static, are utilized, both demonstrating consistent performance in evaluating thermal characteristics. The study also addresses the importance of accounting for nonlinearity in thermal conductance due to temperature dependency, which is essential for accurate thermal characterization. Additionally, it explores the potential for measuring the Thermal Impedance between Junction and Case in power modules without a baseplate, offering a comprehensive understanding of thermal performance.

**KEYWORDS** Thermal Impedance Characterization, IGBT Module Reliability,Virtual Junction Temperature Measurement, Thermoelectric Characterization

## **I. INTRODUCTION**

Applications have evolved significantly and become increasingly complex, spanning from power generation, transmission, and distribution to end consumers. In recent years, advancements in the automotive and aerospace industries have steered projects in new directions, with reliability becoming a key design factor. For instance, research conducted by the European Center for Power Electronics (ECPE) involved over 81 designers from the European Union, revealing that electronic converter applications have an expected lifespan of over 10 years [\[1\]](#page-9-0).

Historical failure records indicate that power semiconductor modules and capacitors are the most vulnerable components in power systems. This vulnerability is due to the wide range of applications and stressors, such as high operating temperatures, thermal cycling, dust, vibration, radiation, and electromagnetic interference [\[1\]](#page-9-0).

Reliability is a critical performance factor that must be considered during the design, manufacturing, and field operation of power converters [\[2\]](#page-9-1). Research on the reliability of electronic converters has been conducted both by industry and by academia, and it primarily divides into two main branches. The first branch focuses on conditioning methods of devices to predict failures and monitor their degradation. The second branch involves fault tolerance, ensuring that the converter continues to operate even after the failure of a component through redundancy systems [\[3\]](#page-9-2).

The current work is an extension of [\[4\]](#page-9-3), incorporating the measurement of Thermal Impedance  $(Z_{th})$  using two different methods, comparing the results both with each other and with the manufacturer values. Additionally, it addresses the measurement of the Virtual Junction Temperature  $(T_{vi})$  using the Thermo Electric Sensitive Parameter (TSEP) method and presents an approach for measuring  $Z_{th}$ between the junction and the case in IGBT modules without a baseplate—information that is not available in datasheets for such modules due to the difficulty of the measurements. This study is essential for assessing the lifespan of modules in type testing, qualification, and practical applications, as  $Z_{th}$  is typically measured during these tests.

This paper is organized as follows: Section II explores IGBT losses, encapsulation techniques, main failure modes, and electrothermal characterization. In Section III, the experimental methodology is detailed, including the approaches, tools, and parameters used to conduct the experiments. Section IV presents the experimental findings. Finally, Section V offers concluding remarks, summarizing the key insights of this study and suggesting potential future work.

# **II. THE IGBT MODULE** *A. SWITCHING CHARACTERISTICS*

The IGBT (Insulated Gate Bipolar Transistor) consists of three parasitic capacitors: the capacitor between the Gate and Emitter  $(C_{ge})$ , between the Collector and Emitter  $(C_{ce})$ , and the Miller Capacitor between the Gate and Collector. These parasitic elements arise from the junctions of N-type and P-type materials that make up the IGBT, significantly impacting the device's behavior.

During switching, delays in turn-on and turn-off cause voltage and current to coexist momentarily, as depicted in Fig. [1.](#page-1-0) This overlap results in power dissipation within the switch, leading to switching losses  $(P_{sh})$  [\[5\]](#page-9-4).

Conduction losses  $(P_{cond})$  occur due to non-idealities present throughout the device. These two forms of power dissipation increase the chip temperature, raising the  $T_{vi}$ . Manufacturers specify the Maximum Junction Temperature  $(T_{vjmax})$  in datasheets, which indicates the maximum safe operating temperature for the device. Exceeding this value can result in device failure due to overheating.



<span id="page-1-0"></span>**FIGURE 1. Switching losses in the IGBT due to non-ideal turn-on and turn-off transitions. The figure highlights the energy losses caused by parasitic elements and non-ideal switching behavior. [\[6\]](#page-9-5).**

## *B. PACKAGE CHARACTERISTICS*

The Insulated Gate Bipolar Transistor (IGBT) dissipates power during both switching and conduction. Over time, these power losses cause the chip to heat up. Without proper heat extraction, the chip may reach its  $T_{vjmax}$ , potentially leading to device failure.

Beyond providing mechanical protection for the chip, the primary functions of the encapsulation include creating a pathway for the efficient transfer of heat from the chip to the heatsink and subsequently to the surrounding environment. To fulfill these roles effectively, the encapsulation must be made from materials that ensure both thermal conduction and electrical insulation within the module. The encapsulation comprises various materials, each with distinct thermal and electrical characteristics. Table [1](#page-3-0) provides values for thermal conductivity, coefficient of thermal expansion (CTE), and heat storage of the main materials commonly used in module construction.

Significant differences can be noted in the thermal properties of the materials that constitute the module. For example,



<span id="page-1-1"></span>**FIGURE 2. Cross-section of an IGBT module, showing materials such as silicon for the chip, ceramic for the substrate, copper for the baseplate, and plastic/epoxy for insulation and protection. [\[8\]](#page-9-6).**

the CTE of Silicon (Si) and Copper (Cu) differs by more than four times, meaning that for the same temperature variation, Cu expands four times more than Si.

The switching characteristics of the IGBT induce thermal cycling, leading to alternating heating and cooling cycles within the module. These thermal cycles cause material expansion. However, due to the different CTEs of these materials, varying rates of expansion occur, generating mechanical stress between the layers.

Fig. [2](#page-1-1) illustrates the cross-section of an IGBT module. There are two types of encapsulation used in power modules: those with a baseplate and those without. The latter is often chosen to reduce costs, as it eliminates the need for an additional thick copper layer in the module. This study focuses on power modules without a baseplate, commonly used in various applications, such as Variable Frequency Drive (VSD).

Each layer of the module has a specific function. Bond wires provide electrical connections between chips, within the same package. The Si chip is soldered onto copper to ensure both electrical and thermal conductivity to other points within the package. Copper, in turn, is soldered onto a ceramic plate, typically composed of alumina, providing electrical insulation while maintaining thermal conductivity. The combination of three layers—copper, ceramic, and copper—is referred to as Direct Bonded Copper (DBC). Finally, the DBC is soldered onto a baseplate. When mounted to a heatsink, thermal interface material (TIM) should be used to minimize thermal resistance between the baseplate and the heatsink. It is crucial to ensure that the heatsink surface is clean and free of oxides to maximize heat transfer efficiency. However, in modules without a baseplate, the DBC is in direct contact with the heatsink. Therefore, in these modules, the case temperature is at the DBC point, where there is greater thermal dynamics compared to modules with a baseplate [\[7\]](#page-9-7).

Temperature variations in the IGBT can reach  $\Delta T_{vj}$  of more than 100 K. Therefore, certain parameters previously considered constant need to be reevaluated. For materials such as Si and alumina, a 100 K variation can significantly impact thermal conductivity, which decreases with increas-



<span id="page-2-0"></span>**FIGURE 3. Temperature dependence of thermal conductivity, illustrating how heat conduction decreases as temperature rises. [\[9\]](#page-9-8).**

ing temperature. This hinders heat transfer from the chip to the heatsink. These nonlinear effects are evidenced by experimental results, which show discrepancies compared to simulations due to these nonlinearities. Fig. [3](#page-2-0) illustrates the temperature dependence of thermal conductivity for both materials.

## *C. IGBT FAILURE MODES*

Two predominant failure modes are primarily due to thermomechanical stressors. The encapsulation of IGBTs involves various materials, each with distinct mechanical, electrical, and thermal properties. During operation, thermal stress can lead to fatigue at the interfaces between these materials, affecting the integrity of the solder joints. This constitutes one of the primary failure modes. Solder degradation at these interfaces results in increased Thermal Resistance between the Junction and the Case ( $R_{thJC}$ ), causing the  $T_{vj}$  to rise progressively.

Over time, this fatigue deteriorates the solder joints that bind them, as depicted in Fig. [4.](#page-2-1) This, in turn, elevates the chip's operating temperature, creating a positive feedback loop that accelerates module deterioration and ultimately reduces its lifespan [\[10\]](#page-9-9). In power cycling tests, when the  $R_{th}$  exceeds 20% of its initial value, it is considered that the module has reached the end of its useful life due to solder degradation.

<span id="page-2-1"></span>

**FIGURE 4. Example of deterioration of the solder in a power module. Image obtained by a SAM-type microscope [\[6\]](#page-9-5).**

The second failure mode is related to the bond wires. These internal connection wires within the package are meticulously soldered onto the silicon chip to avoid damaging the die. They are in direct contact with the heat source, subjecting them to significant thermal variations during operation. Consequently, they are susceptible to failures induced by thermal expansion, primarily due to wire bending and CTE incompatibility [\[10\]](#page-9-9).

This failure mode associated with wire fatigue is known as "Liftoff", as illustrated in Fig. [5.](#page-2-2) Due to the higher CTE of the wire compared to that of silicon, stress builds up in this region, ultimately leading to the rupture of the weld between these two materials. This fracture can be detected by monitoring the increase in the saturation voltage  $(V_{\text{cessat}})$ [\[11\]](#page-9-10). Typically, during power cycling tests, if the  $V_{cesat}$ exceeds 5% of its initial value, it is considered that the module has reached the end of its useful life due to wire degradation.



<span id="page-2-2"></span>**FIGURE 5. Liftoff of bond wires in an IGBT due to power cycling, showing degradation and detachment from repeated thermal and mechanical stress [\[12\]](#page-9-11).**

### *D. THERMAL MODEL*

Power modules can be modeled using the concept of  $R_{th}$  and Thermal Capacitance  $(C_{th})$  [\[13\]](#page-9-12). The construction of these modules involves different materials such as semiconductors, metals, ceramics, and metal alloys, each with varying thicknesses and geometries. As a result, each layer has different values of  $C_{th}$  and  $R_{th}$ .

Figure [6](#page-3-1) shows the two predominant models in thermalelectric representations for simulating temperature in power modules. These electrothermal models are represented as electrical circuits, with their respective corrections and limitations.

The Foster model, commonly used, is derived by fitting the  $Z_{th}$  curve provided by manufacturers. Typically, the parameters of the Foster model are given in the form of  $R_{thn}$  and  $\tau_n$ , where each layer of the module is associated with  $n$  index.

On the other hand, the Cauer model is another representation of the package, where each  $R_{th}$  and  $C_{th}$  element is individually associated with a layer of the module. This model has the advantage of allowing knowledge of the

<b>Material</b>	<b>Heat conductivity</b> $\lambda$ [W/(m*k)]	Heat storage characteristics $[kJ/(m^3*K)]$	Thermal expansion coefficient $\alpha$ [10 <sup>-6</sup> /K]
Silicon	148	1650	4.1
Copper	394	3400	17.5
Aluminium	230	2480	22.5
Silver	407	2450	19
Molybdenum	145	2575	
Solders	$\sim 70$	1670	$15-30$
$Al_2O_3$ - DBC	24	3025	8.3
AIN DBC, AIN-AMB	180	2435	5.7
AlSiC $(75\%$ SiC)	180	2223	

<span id="page-3-0"></span>**TABLE 1. Materials used in the package [\[6\]](#page-9-5).**

temperature at each node of the network, unlike the Foster model, which does not have physical significance. It is possible to convert the Foster model to the Cauer model and vice versa, providing flexibility in thermal analyses.

Equation [\(1\)](#page-3-2) describes the main equation for calculating  $Z_{th}$ :

<span id="page-3-2"></span>
$$
Z_{th}(t) = \frac{T_{vj}(t) - T_{ref}}{P} = T_{vj}(t) \circledast^{-1} P(t) \qquad (1)
$$



<span id="page-3-1"></span>**FIGURE 6. a) Foster Model b) Cauer Model [\[6\]](#page-9-5).**

The parameters in [\(1\)](#page-3-2) are defined as follows:  $Z_{th}(t)$ represents the thermal impedance over time,  $T_{vi}(t)$  is the virtual junction temperature,  $T_{ref}$  is the reference temperature,  $P(t)$  is the power dissipation, and  $\otimes^{-1}$  denotes the inverse convolution, which accounts for the dynamic thermal response of the system.

With the parameters  $R_{th_n}$  and  $\tau_n$  for each layer, it is possible to estimate  $T_{vj}$ . The inputs to the model are the losses that occur in the IGBT due to switching and conduction.

### *E. THERMAL CARACTERIZATION*

To achieve an accurate prediction of the  $T_{vj}$  in power modules, such as IGBTs, it is essential to carry out the thermal characterization of the module and use the experimental data obtained to adjust and improve the theoretical models. Thermal characterization plays a crucial role in understanding the thermal behavior of these electronic components, especially in high-reliability systems such as electric vehicle charging infrastructures, where thermal management is vital to ensuring both performance and system longevity [\[14\]](#page-9-13).

This process involves creating a thermal model that accurately represents how heat is generated and dissipated within the device under different operating conditions. In the case of IGBT modules, thermal modeling generally focuses on the heat flow from the active junctions of the IGBT and diode dies to the cooling liquid in the heat sink. Internal elements, such as bonding wires and busbars, are often excluded from the model, as their contribution to heat dissipation is considered minimal compared to the main thermal path.

To validate the thermal model, the simulation results are compared with experimental data, including transient thermal impedance curves provided by the manufacturer. These curves illustrate how the device temperature responds to power dissipation over time and are essential for deriving thermal models suitable for integration into system-level simulations. Obtaining the system thermal impedance curve is crucial for adjusting and refining temperature prediction models in simulations, especially when using the Finite Element Method (FEM). With experimental data, it is possible to make adjustments to the models, providing more accurate predictions of operating temperatures. This allows for more efficient optimization of cooling systems and prevents failures caused by overheating, a critical aspect for applications requiring high reliability.

The heat sink plays a fundamental role in this process by distributing heat more evenly across the module and influencing the thermal coupling between the dies, resulting in overall improvement in thermal management [\[15\]](#page-9-14).

#### **III. EXPERIMENTAL METHODOLOGY**

This section describes the experimental methodology used in the thermal characterization of IGBT modules, with emphasis on its application for detecting the end of life (EOL) of the modules.

### **A.**  $T_{vj}$  **MEASUREMENT METHOD**

Monitoring  $T_{vi}$  is crucial for ensuring the reliability and durability of IGBTs. Effective management of thermal conditions within the converter, facilitated by tracking  $T_{vi}$ ,

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<span id="page-4-0"></span>**FIGURE 7. IGBT NTC and PTC behavior.**

enhances system reliability. Current methods for measuring  $T_{vj}$  can be categorized into three main solutions: optical, physical contact (thermocouples, optical fiber), and TSEP [\[16\]](#page-9-15).

Each method offers distinct pros and cons. Optical methods, such as infrared camera measurements, provide high accuracy but can be costly and impractical for some applications. Physical contact methods, such as thermocouples integrated into the chip, are economically viable but may exhibit slower dynamic responses, potentially missing rapid junction temperature fluctuations [\[17\]](#page-9-16).

The TSEP method capitalizes on the relationship between temperature and voltage derived from semiconductor theory [\[12\]](#page-9-11). The chip itself acts as a thermal sensor, correlating external electrical parameters with temperature. This method is a promising means of quickly acquiring IGBT module temperatures.

The TSEP was chosen due to its simple implementation and applicability to any type of power module. The method involves placing the IGBT into conduction and injecting a small current, typically in the milliampere range, between the emitter and collector. The resulting voltage,  $V_{\text{cesat}}$ , is measured. The IGBT's characteristics vary with temperature and current. Fig. [7](#page-4-0) illustrates the NTC (Negative Temperature Coefficient) and PTC (Positive Temperature Coefficient) regions based on operating current and temperature. For a specific current,  $V_{cesat}$  decreases with increasing temperature in the NTC region and increases in the PTC region [\[18\]](#page-9-17).

By establishing the relationship between  $V_{\text{cesat}}$  and temperature at a specific current, the device can be calibrated to relate  $T_{vj}$  to  $V_{cesat}$ , represented as  $V_{cesat}(T)$ .

The calibration constant is determined using [\(2\)](#page-4-1), which outlines the procedure for calculating this coefficient.

<span id="page-4-1"></span>
$$
\beta_{calibration} = \left| \frac{Vce_{sat2} - Vce_{sat1}}{T_2 - T_1} \right| \tag{2}
$$

Where  $Vce_{sat1}$  represents the value measured at  $T_1$  temperature and  $Vce_{sat2}$  represents the value measured at  $T_2$ , respectively.

#### *B. SQUARE ROOT T METHOD TO*  $T_{vj}$

The Square-Root- $t$  method is a technique designed to enhance the accuracy of junction temperature  $(T_{vj})$  measurements when applied in conjunction with the TSEP technique. This approach is particularly useful for overcoming challenges related to electrical variations and carrier diffusion processes within the semiconductor chip [\[12\]](#page-9-11).

When an IGBT is heated by a high current for a defined period, this transient impacts the value of the collectoremitter voltage  $(V_{ce})$  at the initial moment  $(t = 0)$ , and its influence must be properly adjusted.

This transient needs to be disregarded, and therefore a delay in the measurement of  $V_{ce}$  is applied to mitigate these effects. After this correction, the  $V_{ce}$  curve is adjusted based on [\(3\)](#page-4-2), allowing the extrapolation of the initial junction temperature  $(T_{vi0})$ . This technique assumes that all parameters in [\(3\)](#page-4-2) are constant and establishes a direct relationship between  $T_{vj}$  and the square root of time  $(\sqrt{t})$  during the cooling process [\[19\]](#page-9-18).

<span id="page-4-2"></span>
$$
T_{vj}(t) - T_{vj_0} = \frac{2P}{\sqrt{k}A} \sqrt{t}
$$
 (3)

Moreover, uncertainties in  $T_{vj}$  measurements can introduce significant errors in the estimation of the module's lifes-pan [\[20\]](#page-9-19). Therefore, ensuring accurate  $T_{vj}$  measurements is crucial not only for determining related thermal parameters but also for reliably assessing the module's lifespan.

#### *C.*  $Z_{th}$  **MEASUREMENT**

The experimental determination of  $Z_{th}$  is crucial for the proper sizing of heat sinks, estimating junction temperatures through analytical methods, and predicting the lifespan of modules [\[21\]](#page-9-20). Investigating more precise, simplified, and rapid techniques for obtaining this parameter is essential both for project development and industrial module production, as well as for academic research.

Two techniques for measuring  $Z_{th}$  were analyzed, followed by a detailed discussion of the obtained results in the subsequent subsection.

## 1) DYNAMIC METHOD

The dynamic method for measuring  $Z_{th}$  involves applying power pulses of varying widths to the chip. This approach heats the chip progressively and evaluates its response to each pulse, allowing for the calculation of the  $Z_{th}$  corresponding to the applied pulse width. As discussed in Section III, the module can be represented by a network of thermal capacitors and thermal resistors. The pulse duration causes heat to transfer gradually from the chip to the encapsulation. As the pulse width increases, the internal layers of the module are heated, resulting in a gradual increase in chip temperature. Thus,  $Z_{th}(t = t_{pulse})$  is calculated by knowing the  $T_{vj}$  value reached during the pulse, enabling

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<span id="page-5-0"></span>**FIGURE 8. Behavior of**  $V_{cesat}$  for different heating pulse widths. Due to module heating, the  $\Delta V_{ce}$  increases, highlighting the effect of **temperature on the saturation voltage.**

the construction of the thermal impedance curve point by point and the analysis of specific regions of the module [\[22\]](#page-9-21).

For instance, to specifically analyze the solder between the chip and the DBC, a short pulse can be used to predominantly heat that region. Fig. [8](#page-5-0) illustrates the behavior of  $V_{cesat}$  after applying pulses of different widths to the module, all scaled to the same time interval. It is observed that the larger the pulse width, the greater the  $\Delta V_{ce}$ , indicating more significant heating of the module. After the pulse,  $V_{ce}$ begins to increase until it returns to its pre-pulse reference value, due to the NTC behavior of the module.

Therefore,  $Z_{th}$  can be calculated for the specific pulse value using [\(1\)](#page-3-2). However, it is crucial to adjust  $T_{\nu j0}$  using the Square Root t method for each pulse.

## 2) STATIC METHOD

The static method for determining  $Z_{th}$  involves applying a single power pulse long enough for the modules  $T_{vj}$  to reach a steady-state condition, where the module achieves thermal equilibrium before power supply interruption.

After applying the power pulse for a sufficient time to reach thermal equilibrium, switch S1 is opened, cutting off power to the module. Following this, the cooling curve is monitored, which represents the variation in junction temperature over time after the power pulse has been interrupted. This variation is recorded through continuous measurement of  $V_{ce}$ , which reflects changes in  $T_{vj}$  during the cooling process. Equation (1) is applied to all recorded points, making it possible to acquire the complete response of  $Zth$ with just a single, sufficiently long power pulse.

Analyzing the cooling curve provides insights into the module's heat dissipation and thermal impedance. By evaluating the module's response to the pulse, one can gain a comprehensive understanding of its thermal characteristics, which is crucial for optimizing heat sink design and improving the module's thermal management.



**FIGURE 9. Setup for experimental tests.**

<span id="page-5-1"></span>

<span id="page-5-2"></span>**FIGURE 10. Circuit Diagram for tests [\[23\]](#page-9-22)**

#### **IV. EXPERIMENTAL RESULTS**

Experimental results are presented in this section, where the module is calibrated to find the constant that relates  $Vce_{sat}$ with  $T_{vj}$  for low current, along with the experimental methods for obtaining  $Z_{th}$  using static and dynamic approaches.

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The experimental arrangement used to obtain the results is partially depicted in Fig. [9.](#page-5-1) The Chroma 62012P-40-120 power supply is employed to provide a constant current and induce heating of the module. An electronic load applies a fixed current of 100 mA for the measurement of  $V_{\text{cesat}}$ . The auxiliary switch controls the pulse width, which is defined by the Programmable Logic Controller (PLC). Ambient temperature is measured using a Fluke 1587, while the MSO44 oscilloscope performs dynamic readings of  $V_{\text{cesat}}$ . The GP20 data collector, along with the GX90XA-04-H0N-3N module, is used to read type T thermocouples placed on the case and heatsink of the Device under Test (DUT). Additionally, the Tektronix TPS2014B oscilloscope is used for other measurements.

This setup ensures accurate measurement of thermal parameters and junction temperatures, facilitating a reliable comparison between experimental data and numerical simulations.

Fig. [10](#page-5-2) illustrates the basic circuit configuration used for conducting the tests. In this setup, the PLC manages the duration for which switch S1 remains closed, allowing the load current (*ILoad*) to heat the DUT. Upon opening switch S1, the collector voltage  $V_{ce}$  is recorded using a sensing current (Isense). It is important to highlight that the S1



<span id="page-6-0"></span>**FIGURE 11. IGBT calibration curve obtained experimentally using temperature chambers.**

key should be as fast as possible. The use of MOSFETs for this activation is recommended due to the switching characteristics of this device. The gate-emitter voltage used in the DUT was 15V.

### **A.**  $T_{vj}$  **MEASUREMENT METHOD**

As discussed in section III, measuring  $T_{vj}$  sing the TSEP method requires establishing a relationship between  $Vce_{sat}$ and  $Tvj$ .

By establishing the relationship between  $V_{\text{cesat}}$  and temperature at a specific current, the device can be calibrated to relate  $T_{vj}$  to  $V_{cesat}$ , represented as  $V_{cesat}(T)$ .

Figure [11](#page-6-0) displays the calibration curves for the IGBT used in our tests. These curves exhibit excellent linearity. It is crucial to emphasize the importance of both the accuracy and stability of the current source. Even minor variations in current can significantly affect  $V_{\text{cesat}}$ , given the nature of the relationship, which is on the order of  $\frac{mV}{K}$ .

When  $Vce_{sat1}$  represents the value measured at  $T_1$  temperature and  $Vce_{sat2}$  represents the value measured at  $T_2$ , respectively.

Tests were conducted on the Infineon IGBT model FP30R12W1T7 within a Termotron climate chamber. As anticipated, the calibration coefficient was determined to be 1.99  $mV/K$ .

Calibration is essential due to inherent variations in the module manufacturing process. Therefore, a constant calibration coefficient cannot be assumed across different semiconductor batches.

Using the TSEP method, the cooling curve of a module can be determined. Assuming the cooling curve is the conjugate of the heating curve under consistent conditions, mathematical transformations can convert the cooling curve into the corresponding heating curve, allowing the calculation of  $Z_{th}$  and providing precise data on the module's thermal dissipation [\[24\]](#page-9-23).

Fig. [12](#page-6-1) displays the cooling curves on a logarithmic time scale for different heating power values. A logarithmic scale is used for transient thermal analysis to understand



<span id="page-6-1"></span>**FIGURE 12. Junction Temperature for Different Heating Values.**



<span id="page-6-2"></span>**FIGURE 13. Correction of heating pulses using the Square-Root-t-Method** for measuring  $T_{vi}$ .

curve evolution better. Within the first 10 ms, temperature variation is minimal. Between 10 ms and 100 ms, the curve shows more pronounced changes. After 100 ms, the curve smooths out, with a change in concavity until reaching room temperature.

#### *B. SQUARE ROOT T METHOD TO*  $T_{vj}$

In section III, it was discussed that the TSEP method for measuring  $T_{vj}$  requires a correction due to the transient, because when switch S1 is opened and the ILoad is reduced to zero, leaving only the Isense in the circuit, a transient is generated.

A delay (td) of approximately 400 µs is applied to the measurement of  $V_{ce}$  to mitigate these effects. Following this, the  $V_{ce}$  curve is adjusted based on, allowing the extrapolation of the initial junction temperature  $(T_{vj0})$ .

Fig. [13](#page-6-2) illustrates the curve obtained for different pulse widths and the corresponding adjustment curves. It is observed that a larger pulse width results in a higher measured value of  $T_{vi0}$ .

#### *C. MEASURE*  $Z_{th}$  *in MODULES WITHOUT BASEPLATE*

When measuring the  $T_{vi}$ , the Case Temperature  $(T_c)$ , and the Heatsink Temperature  $(T_h)$  during the application of a long power pulse, it is observed that the thermal dynamics at each of these points differ significantly. These differences have important implications for the calculation of  $Z_{th}$ . Fig. [14](#page-7-0) illustrates the corresponding temperature curves.

The analysis of the curves reveals that the rate of change of  $T_{vj}$  is significantly higher, while  $T_h$  remains practically constant during the pulse application. This is due to the large thermal reservoir of the heatsink, which dampens thermal variations. As a result, when calculating the Thermal Impedance between the Junction (J) and the Heatsink (H)  $(Z_{thJH})$ , the expected behavior is observed [\[25\]](#page-9-24).

Upon analyzing the dynamics of the  $T_c$ , it is noted that its rate of change is slower than that of  $T_{vj}$ , but it exhibits a significant temperature variation. The Fig. 15 shows an increase in  $T_c$  while  $T_{vj}$  has already reached a steady state. This behavior introduces an anomaly in the calculation of the Thermal Impedance between the Junction and the Case(C)  $(Z_{th,IC})$  due to this delay.

As can be observed in Fig. 16, there is a region of the curve  $Z_{thJC}$  where it decreases over time. This occurs because, at the moment when  $T_{vj}$  is already in thermal equilibrium,  $T_c$  is still increasing. When calculating  $Z_{thJC}$ using (1), it is possible to detect that the value decreases due to the discrepancy between  $T_c$  and  $T_{vj}$  resulting in this anomalous behavior, in both methods we have the same behavior. This is different from  $Zth_{JH}$ , where  $T_h$  remains practically constant throughout the measurement.

Typically, modules without a baseplate do not provide the  $Z_{thJC}$  value in their datasheets due to the observed differential thermal behavior. In modules without a baseplate, the thermal interaction between the  $T_{vj}$  and the  $T_c$  can be complex. On the other hand, datasheets often provide the  $Z_{thJH}$  value, as the heatsink usually has a more predictable and stable thermal behavior compared to the case.

Figure [15](#page-7-1) displays the thermal impedance curves between the junction and heatsink, and the junction and case, using both measurement methods. The two techniques show that  $Z_{thJH}$  is stable, as  $T_h$  remains nearly constant throughout the pulse, serving as a reference value. In the  $Z_{thJC}$  curve, there is a noticeable dip where  $Z_{th}$  decreases in a region of the curve. This decrease occurs because  $T_{vi}$  is already fixed while  $T_c$  continues to rise, causing  $Z_{thJC}$  to decrease. This anomalous behavior is observed in both techniques.

There exists a region in Fig. 16 where the  $Z_{thJC}$  and  $Z_{thJH}$  curves align and then begin to diverge. In both techniques, this region is around 100 ms. It can be inferred that from  $t = 0$  to  $t = 100ms$  this region is associated with internal heating within the module, where  $T_c$  and  $T_h$  are constant while only  $T_{vj}$  is increasing. The region where the divergence begins represents the actual value of he  $Z_{thJC}$ .



<span id="page-7-0"></span>**FIGURE 14. Temperature of a module without a baseplate, showing that**  $T_{vi}$  varies more rapidly compared to the  $T_c$ , while the  $T_h$  remains nearly **constant throughout the pulse.**



<span id="page-7-1"></span>**FIGURE 15. Thermal impedance of a module without a baseplate shows** that  $Z_{th,IC}$  and  $Z_{th,IH}$  start nearly identical during heating and diverge, with the divergence point indicating the value of  $Z_{th,IC}$ .

## *D.*  $Z_{thJH}$  with different values of power

Figure [12](#page-6-1) displays the cooling curves of  $T_{vi}$  for different power levels while maintaining the same pulse duration. Significant variations in  $T_{vj}$  are observed for pulses of 15W, 30W, and 50W. For a 50W pulse,  $T_{vj}$  exceeded 120°C, whereas, for a 15W pulse,  $T_{vi}$  reached approximately 50°C. The more than 70°C difference in  $\Delta T_{vj}$  directly impacts the value of  $Z_{th}$  due to the high-temperature dependence of silicon's thermal conductivity. This affects the system's heat dissipation capability.

Figure [16](#page-8-0) shows the  $Z_{thJH}$  values corresponding to different power levels. It is observed that for lower power levels, the thermal impedance is also lower. This behavior is associated with thermal variations in the package materials, reflecting the dependency of thermal impedance on the thermal operating conditions of the device.

Figure [17](#page-8-1) presents a comparison between the static and dynamic methods for determining thermal impedance relative to the values specified in the component datasheet. It is



<span id="page-8-0"></span>FIGURE 16.  $Z_{thJH}$  for different power levels using the Static Method.Due to the increased heating of the materials with higher power pulses,  $Z_{thJH}$ **is greater, as thermal conductivity decreases with rising temperature.**



<span id="page-8-1"></span>**FIGURE 17. Comparison of Static and Dynamic Methods with datasheet results. Both methods exhibit similar behavior and show good agreement.**

observed that the curves obtained from both methods show good overlap, indicating consistency in  $Z_{thJH}$  measurements when both methods are employed.

However, discrepancies compared to datasheet values can be attributed to several factors. These include the safety margin adopted by the manufacturer, the heat dissipation method used (in this case, only the heatsink), and variations in thermal impedance measurement methods.

Datasheet values often represent an average of multiple modules tested under conditions and methods that may differ from those applied in this study. It is known that some manufacturers use more sophisticated heat dissipation systems, such as water-cooled heatsinks, for thermal impedance testing. These methods may result in different  $Z_{thJH}$  values compared to those obtained with conventional methods.

This approach highlights the importance of considering specific measurement conditions and test methods when interpreting and comparing thermal impedance data across different studies and manufacturer specifications.

### **V. CONCLUSION**

In this study, two primary methods for measuring the  $Z_{th}$ of power modules were investigated and compared: the static method and the dynamic method. Each method has distinct characteristics and provides valuable insights into the thermal behavior of the devices.

The static method involves applying a single, sufficiently long power pulse to allow the  $T_{vj}$  to reach a steady state, followed by analyzing the complete cooling curve after power removal. In contrast, the dynamic method uses multiple power pulses of varying widths to analyze the thermal impedance curve point by point, which is crucial for evaluating the thermal response in different regions of the module.

Both methods have their advantages and disadvantages. The static method, with its simplified approach, facilitates the analysis of steady-state thermal behavior but may not fully capture the transient behavior of the module. The dynamic method, while providing a more detailed view, may face challenges in data interpretation and identification of critical areas due to the complexity of the tests.

Non-linearity in the thermal conductance of materials, especially due to temperature dependence, is another critical consideration during these tests, as it can significantly impact heat dissipation and, over the long term, the lifespan of components.

Obtaining accurate  $Z_{th}$  curves is fundamental not only for thermal characterization and reliability estimation but also for improving theoretical electrothermal models. Precision in determining these curves allows for better adjustments of theoretical equations, resulting in more accurate and reliable temperature predictions.

Additionally, the study revealed an approach to estimate the value of  $Z_{thJC}$  based on the region of separation between the  $Z_{thJH}$  and  $Z_{thJC}$  curves. This estimation is particularly valuable, as information on  $Z_{thJC}$  is often not provided in datasheets due to the challenges associated with the simultaneous measurement of  $T_c$  and  $T_{vj}$ . The ability to estimate  $Z_{thJC}$  based on curve analysis offers a solution to the lack of data and enhances the understanding of the thermal characteristics of this kind of module that does not have a baseplate.

For future work, a statistical approach utilizing multiple modules could be employed to verify the dispersion of  $Z_{th}$ values. The study could also be extended to larger power modules, with experimental results replicated in simulation models.

## **AUTHOR'S CONTRIBUTIONS**

D. F SOUZA: Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Project Administration, Resources, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. D. S. GREFF: Formal Analysis, Methodology,

Supervision, Validation, Visualization, Writing – Original Draft, Writing – Review  $\&$  Editing.

### **PLAGIARISM POLICY**

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

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